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A Robust Multilevel Inverter Topology for Operation under Fault Conditions

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Abstract: Multilevel inverters (MLIs) are used on a large scale because they have low total harmonic distortion (THD) and low voltage stress across the switches, making them ideal for medium- and high-power applications. The authenticity of semiconductor devices is one of the main concerns for these MLIs to operate properly. Due to the large number of switches in multilevel inverters, the possibility of a fault also arises. Hence, a reliable five-level inverter topology with fault-tolerant ability has been proposed. The proposed topology can withstand an open-circuit (OC) fault caused when any single switch fails. In comparison to typical multilevel inverters, the proposed topology is fault-tolerant and reliable. The simulation of the proposed topology is conducted in MATLAB-Simulink and PLECS software packages, and the results obtained for normal pre-fault, during-fault, and after-fault conditions are discussed. Experimental results also prove the proposed cell topology's robustness and effectiveness in tolerating OC faults across the switches. Furthermore, a thorough comparison is provided to demonstrate the proposed topology's superiority compared to recently published topologies with fault-tolerant features.

Keywords: packed U-cell (PUC); fault-tolerant; self-voltage balancing; reduced device count; total harmonic distortion (THD); modulation index

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1. Introduction

An ever-increasing demand for electrical energy has resulted in the severe depletion of traditional energy sources, which has led to large-scale research into a renewable energy source (RES)-based power generation. New power converter technologies are necessary for intended operation, control, and power management in order to increase power quality. Multilevel inverters were first introduced in early 1975 [1]. These MLIs are becoming increasingly popular due to their high voltage operation ability, higher efficiency, lower switching losses, and lesser electromagnetic interference [2]. MLIs are one of the best options to fulfill the increasing demand for power. MLIs can produce staircase-like AC voltage by the unique connections of switches with DC sources [3]. Due to these advantages, MLIs are widely used in place of two-level inverters.

To increase efficiency, the total harmonic distortion (THD) of the inverter must be decreased. The square-wave output contains an infinite number of harmonics, and to reduce this, we must make multilevel level output that is close to the sinusoidal waveform with reduced harmonics in the output voltage. Multilevel inverters can be of the 2n + 1 type, where n is an integer [4]. A multilevel inverter requires more switches, increasing the possibility of switching failure, and therefore, the unbalanced output voltage is obtained,

causing increased THD in the output voltage. Inverters, based on the source, are of two types [1]: (1) the current source type and (2) the voltage source inverter. Based on the source type, a multilevel inverter is further classified as (1) a single DC source or (2) a multiple DC source. In a single DC source multilevel inverter, there are two types: the first is asymmetric, meaning the DC sources' voltage across the terminal is equal, and the second is asymmetrical, meaning the voltage across the terminal is unequal. The above classification of the inverter is provided in Figure 1.

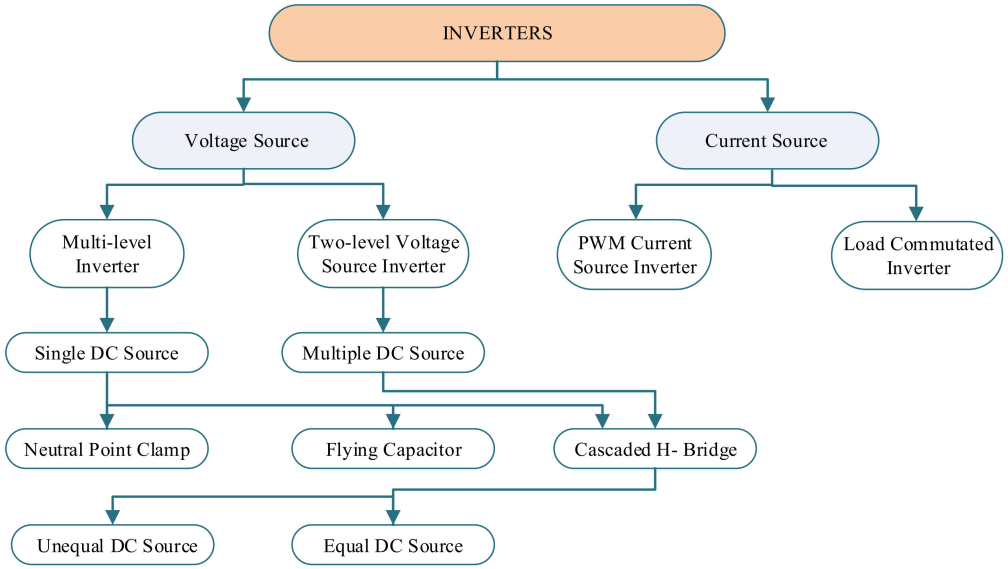


Figure 1. Classification of multilevel inverters.

The well-known conventional topologies of the multilevel inverter are used in different industrial applications due to the unique features of these topologies; however, they need a significant number of the fundamental components of MLIs, such as switches, DC power supplies, capacitors, and diodes, as we are moving towards higher voltage levels. A comparison of the fundamental component of conventional topologies is provided in Table 1 [5], where t is the number of levels. Flying capacitors use additional capacitors, which are clamped across the switches to produce extra voltage. The diode-clamped inverter uses a clamp diode along with a capacitor to produce multilevel output voltage. Flying capacitors, and diode-clamped MLIs, have the disadvantage of needing many capacitors and diodes to produce higher levels. In contrast, cascaded H-bridge inverters contain multiple, separate DC sources and many power semiconductor devices for generating higher levels, and external circuits are required to maintain the capacitor voltage. They also create the problem of unbalancing capacitor voltage in addition to the incapability of self-voltage boosting.

Table 1. Comparison of component count for conventional topologies.

Inverter Configuration	Diode-Clamped	Flying Capacitor	Cascaded Inverter
Switches	$2(t-1)$	$2(t-1)$	$2(t-1)$
Main Diodes	$2(t-1)$	$2(t-1)$	$2(t-1)$
Clamping Diodes	$(t-1)(t-2)$	0	0
DC Bus Capacitor	$(t-1)$	$(t-1)$	$(t-1)/2$
Balancing Capacitor	0	$(t-1)(t-2)/2$	0

MLIs have low reliability, which is the main area of concern, and this low reliability is due to the power switches that are most vulnerable in nature, but in reality, we use more devices due to the above-mentioned advantages, and this opens the possibility for

researchers to reduce the device count. Again, there is a problem when using a smaller number of power switches and redundant path reduction for uninterrupted system use because we have to make the system fault-tolerant. Multiple open-circuit faults are a possible scenario. In this paper, we will study what happened after fault operation due to a fault in a single switch of the circuit. MLIs are used in different applications, including machine drives and renewable-energy conversion such as photovoltaic systems, and these applications require an undisturbed, continuous, and protected mode of application. As a result, we require robust and reliable power inverters, which are essential for maintaining the power supply [6]. The literature in [7] looked into post-fault operation and topologies. In terms of fault-tolerant operations, the previous works of literature have presented a variety of methodologies. Several fault operation methods are classified into four categories. The first solution involves redundant operation. In the second solution, the fundamental concept of the leg-level is to provide redundant legs in the parallel or series connections to the main legs, where the redundant parallel leg offers a better combination of system cost and performance. In the third solution, a module of the multilevel inverter is used, such as cascaded-H bridge (CHB) modular multilevel converters (MMCs), for making the circuit fault-tolerant. Lastly, in the fourth solution, redundant series or parallel converters are used to tolerate the fault. Several techniques have been used to extend the lifetime of long-run power devices, including cooling devices [8], power derating [9], and modulation method reconfiguration. However, these approaches fail when the switch is utterly wrecked; in this situation, only topology reconfiguration works.

The remaining paper is laid out as follows. In Section 2, the five-level fault-tolerant topology is proposed. Section 3 presents the conventional NLC applied to the proposed inverter. In Section 4, power loss analysis is performed on the proposed inverter. Sections 5 and 6 provide the simulation verification and experimental validation of the discussed inverter, respectively. In Section 7, a comparison between similar inverter topologies is presented. Section 8 concludes the paper.

2. Proposed Five-Level Fault-Tolerant MLI Topology

The proposed topology in this paper consists of nine active switches and two isolated DC sources, where the second source is fixed at half of the first DC source as shown in Figure 2. Switches S_7, $S_{8,}$ and S_9 are added to this circuit to provide more redundant paths for each output voltage level. As the number of redundant paths increases, the circuit has additional paths to obtain the required voltage if there is a fault in any switch of the circuit. The proposed five-level topology counters the drawback of experiencing a complete shutdown during the failure (OC) in switches S_1 and S_4. The output voltage level reduces to three-level during the failure in switches S_2 and S_3. The switching table of the proposed topology is provided in Table 2. Table 3 shows the potential switching states and viable output voltage levels if any switch from S1 to S9 fails (OC fault), taking one switch faulty at a time. As an example, if switch S_1 fails, all of the five levels can be synthesized using one of the modes for each level from δ_2, δ_3, δ_4, δ_5, δ_8, δ_9, δ_{12}, δ_{13}, δ_{14}, δ_{15}, δ_{16}, δ_{17}, δ_{18}, δ_{19}, and $\delta_{20,}$ as shown in Figure 3.

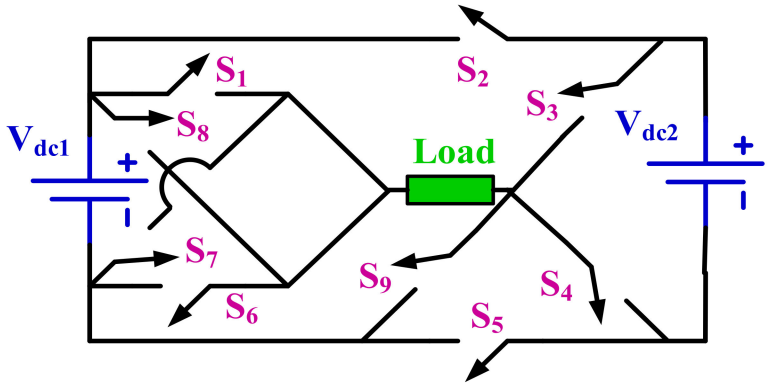


Figure 2. Proposed five-level fault-tolerant topology.

Table 2. Switching table of proposed five-level fault-tolerant topology.

Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9
0	1	1	1	0	0	0	0	0	0
	0	0	0	1	1	1	0	0	0
	0	1	1	0	0	0	0	1	0
	0	0	0	0	0	0	0	1	1
	0	0	0	0	1	1	1	0	0
V_{dc2}	1	1	0	0	0	1	0	0	0
	0	1	0	0	0	1	0	1	0
$(V_{dc1} - V_{dc2})$	1	0	1	0	1	0	0	0	0
	0	0	1	0	1	0	0	1	0
V_{dc1}	1	0	0	0	0	0	0	0	1
	1	0	0	0	1	1	0	0	0
	0	0	0	0	1	1	0	1	0
	0	0	0	0	0	0	0	1	1
$-V_{dc2}$	0	1	0	0	0	1	1	0	0
	0	0	1	0	1	0	1	0	0
	0	0	1	1	1	0	0	0	0
	0	1	0	0	0	1	1	0	0
$-(V_{dc1} - V_{dc2})$	0	1	0	1	0	1	0	0	0
$-V_{dc1}$	0	1	1	1	0	0	0	0	0
	0	1	1	0	0	0	0	1	0

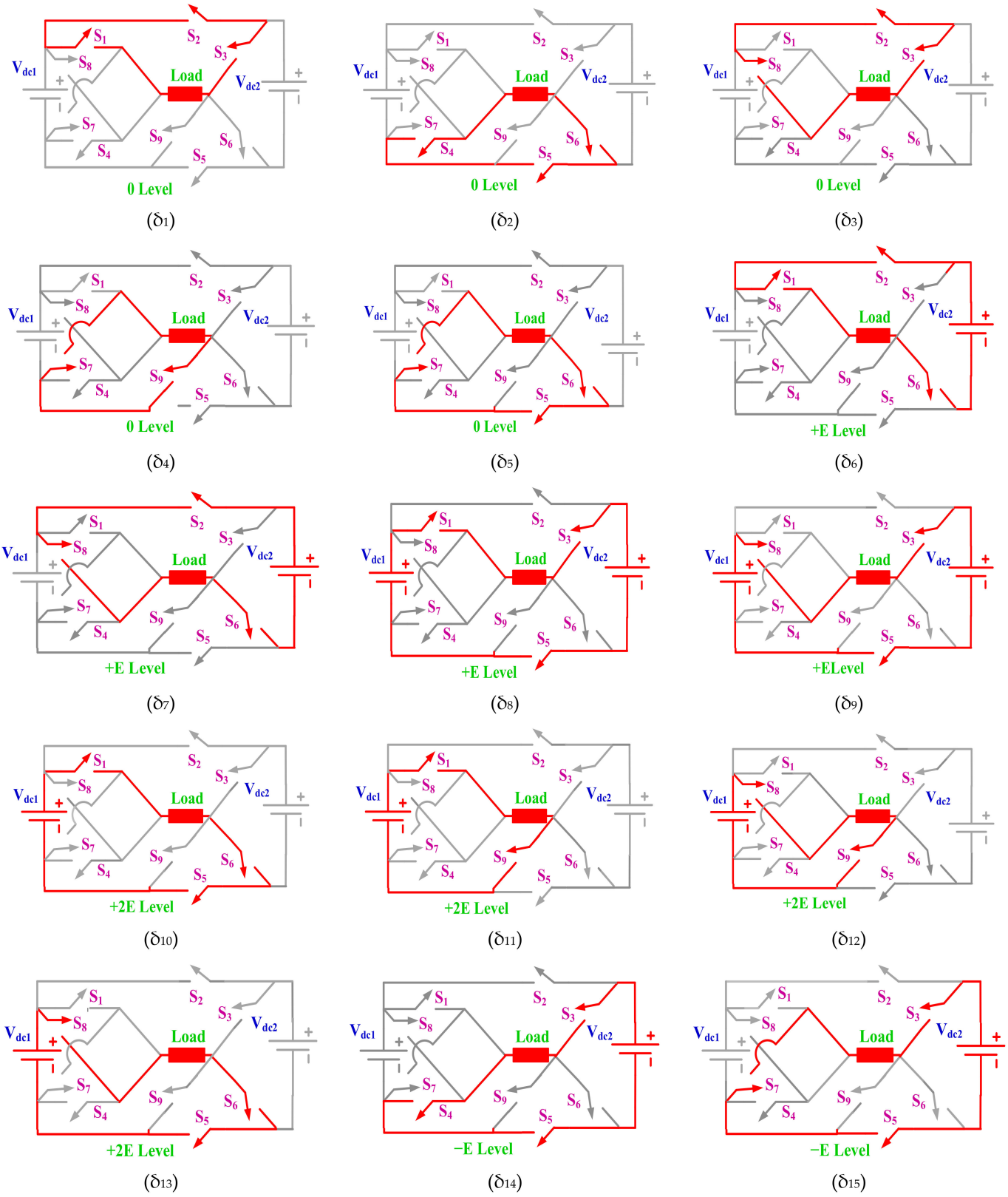


Figure 3. *Cont.*

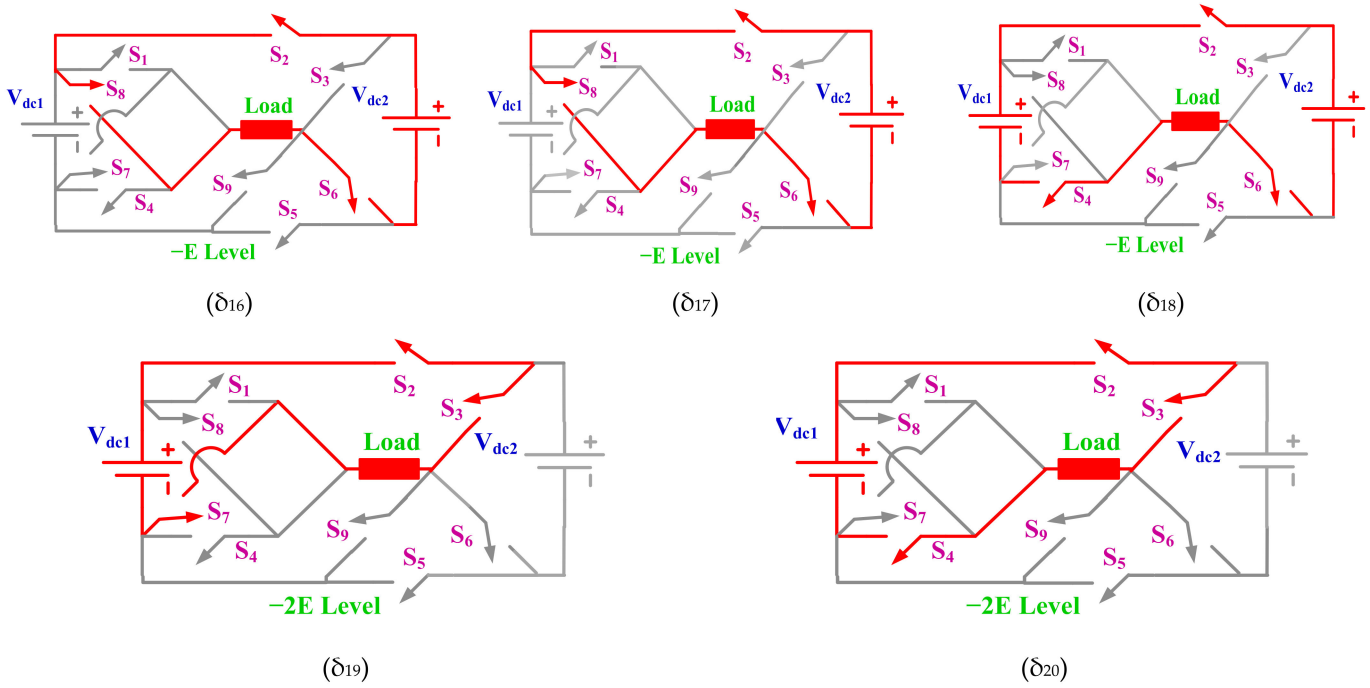


Figure 3. All twenty switching states of proposed five-level fault-tolerant topology.

Table 3. Different modes for any single switch OC fault in proposed five-level fault-tolerant topology.

Failed Switch	Available Modes	Operation Level
S_1	$\delta_2, \delta_3, \delta_4, \delta_5, \delta_8, \delta_9, \delta_{12}, \delta_{13}, \delta_{14}, \delta_{15}, \delta_{16}, \delta_{17}, \delta_{18}, \delta_{19}, \delta_{20}$	5
S_2	$\delta_2, \delta_3, \delta_5, \delta_7, \delta_9, \delta_{10}, \delta_{13}, \delta_{12}, \delta_{13}, \delta_{14}, \delta_{15}, \delta_{16}, \delta_{17}, \delta_{18}, \delta_{19}, \delta_{20}$	3
S_3	$\delta_1, \delta_3, \delta_4, \delta_5, \delta_6, \delta_7, \delta_8, \delta_9, \delta_{10}, \delta_{11}, \delta_{12}, \delta_{13}, \delta_{14}, \delta_{16}, \delta_{18}$	3
S_4	$\delta_1, \delta_3, \delta_4, \delta_5, \delta_6, \delta_7, \delta_8, \delta_9, \delta_{10}, \delta_{11}, \delta_{12}, \delta_{13}, \delta_{14}, \delta_{16}, \delta_{18}$	5
S_5	$\delta_1, \delta_4, \delta_5, \delta_6, \delta_8, \delta_{10}, \delta_{11}, \delta_{13}, \delta_{14}, \delta_{15}, \delta_{16}, \delta_{18}, \delta_{19}, \delta_{20}$	5
S_6	$\delta_1, \delta_4, \delta_5, \delta_7, \delta_9, \delta_{10}, \delta_{13}, \delta_{15}, \delta_{17}, \delta_{19}, \delta_{20}$	5
S_7	$\delta_1, \delta_2, \delta_4, \delta_6, \delta_7, \delta_8, \delta_9, \delta_{10}, \delta_{11}, \delta_{12}, \delta_{13}, \delta_{15}, \delta_{18}, \delta_{19}$	5
S_8	$\delta_1, \delta_2, \delta_3, \delta_5, \delta_6, \delta_7, \delta_{10}, \delta_{11}, \delta_{14}, \delta_{15}, \delta_{16}, \delta_{17}, \delta_{18}, \delta_{19}, \delta_{20}$	5
S_9	$\delta_1, \delta_2, \delta_3, \delta_4, \delta_6, \delta_7, \delta_8, \delta_9, \delta_{11}, \delta_{12}, \delta_{14}, \delta_{15}, \delta_{16}, \delta_{17}, \delta_{18}, \delta_{19}, \delta_{20}$	5

3. Conventional Nearest Level Control (NLC)

Modulation techniques play a crucial role in affecting switching loss, harmonics, and filter size. Conventional modulation methods have higher complexity, high switching loss, and increased switching harmonics as the number of submodules increases. The NLC has the advantage of low switching losses and minimum low order harmonics for higher output voltage applications. In the conventional NLC technique, a sinusoidal signal is used as a reference (V_{ref}) signal, as shown in Figure 4 [10], which is compared with other carrier signals (B1 to Bn). The conventional procedure is presented in [11]. In this, $0.5V_{dc}$ DC loss error is always maintained between two levels. The working principle is depicted in Figure 5.

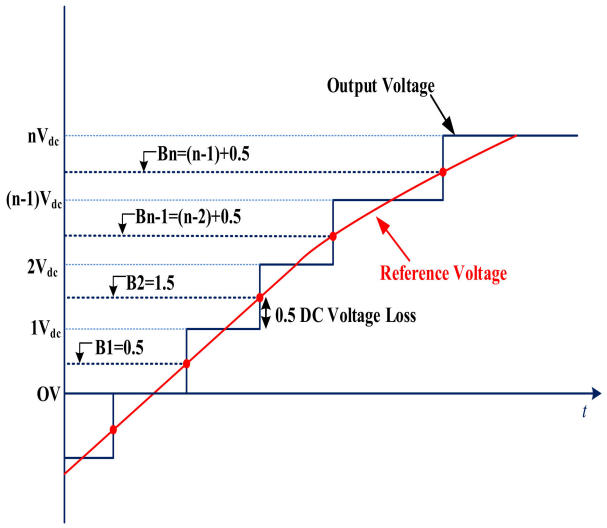


Figure 4. Level generation.

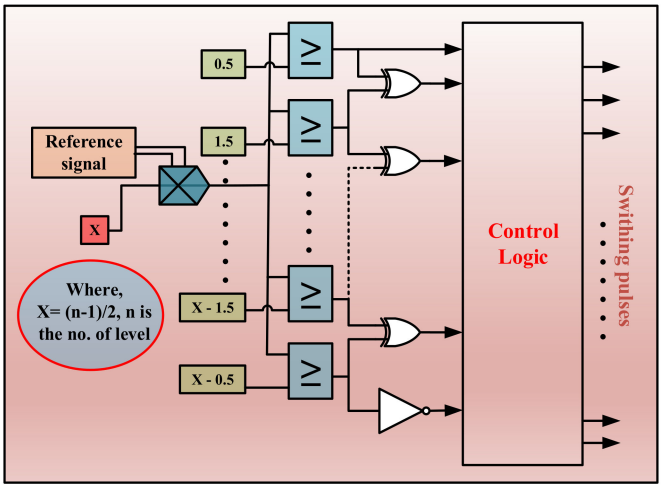


Figure 5. Simplified NLC.

For N levels:
The total number of carrier signals (B_1 to B_n) is expressed as

$$\begin{array}{cccccccc} B_1 & B_2 & B_3 & B_3 & \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots & B_{n-1} & B_n \\ 0.5 & 1+0.5 & 2+0.5 & 3+0.5 & & (n-2)+0.5 & (n-1)+0.5 \end{array}$$

where $n = (N_{level} - 1)/2$.
The output voltage is

$$V_{out} = m * \frac{N_{level} - 1}{2} * V_{dc} * \cos(\omega t)$$

where m refers to the modulation index and is expressed as

$$m = V_{ref}(max)/nV_{dc} \quad (1)$$

The switching angles for the conventional NLC are given by

$$\theta_j = \sin^{-1}[(j - 0.5)/n] \quad (2)$$

where j = 1, 2, 3 . . . . . $(N_{level} - 1)/2$.

4. Power Loss Analysis

PLECS software has been used to calculate the power loss and efficiency, and the software's thermal modelling is used to correctly determine conduction and switching losses for all switches. Infineon's IGBT switch IGA30N60H3 was chosen for this investigation. Figure 6 depicts the IGBT's turn on, turn off, and conduction loss models, respectively, and two types of losses were considered, i.e., the switching losses (P_S) and conduction losses (P_C) of all the semiconductor devices.

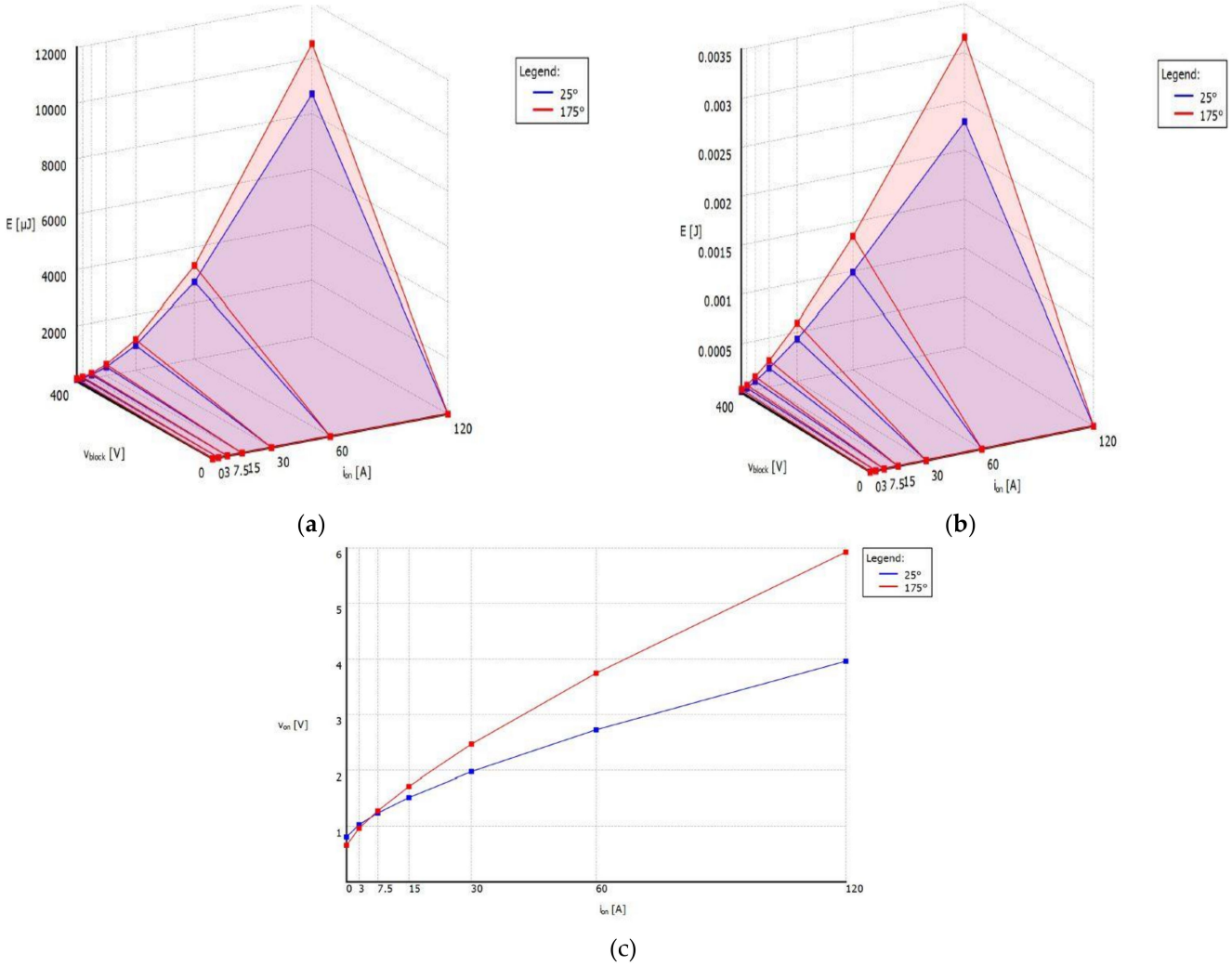


Figure 6. (**a**) Turn on loss, (**b**) turn off loss, and (**c**) conduction loss.

4.1. Switching Losses (P_S)

Switching losses occur when the switches turn on or off [12,13]. Switching losses can be calculated by using the equations below.

The power loss during the interval of switching on is expressed by

$$P_{S,\,on,\,n} = f\int_0^{t_{on}} v(t)i(t)dt = f\int_0^{t_{on}} \left(\frac{V_{S,n}}{t_{on}}t\right)\left(-\frac{I_n}{t_{on}}(t-t_{on})\right)dt = \frac{1}{6}\,f\,V_{S,n}I_n t_{on}$$

The power loss during the interval of switching off is expressed by

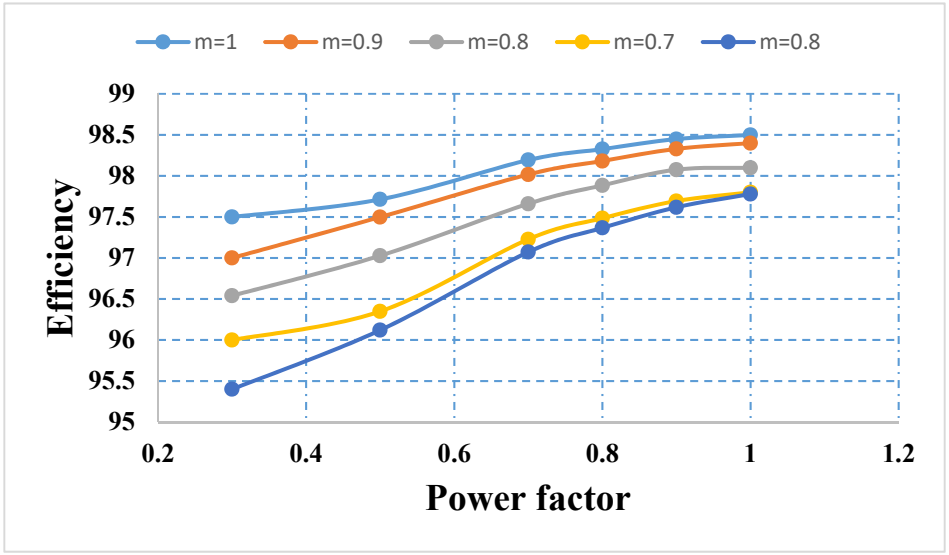
$$P_{S,\,off,\,n} = f\int_0^{t_{off}} v(t)i(t)dt = f\int_0^{t_{off}} \left(\frac{V_{S,n}}{t_{off}}t\right)\left(-\frac{I_n'}{t_{off}}\left(t-t_{off}\right)\right)dt = \frac{1}{6}\,f\,V_{S,n}I_n' t_{off}$$

where I_n and I_n', respectively, signify currents across the nth switch when it was turned on and before it was turned off. $V_{S,n}$ specifies the voltage for the off-state of the nth switch, and f denotes the switching frequency. The on and off losses are summed to calculate the total switching loss:

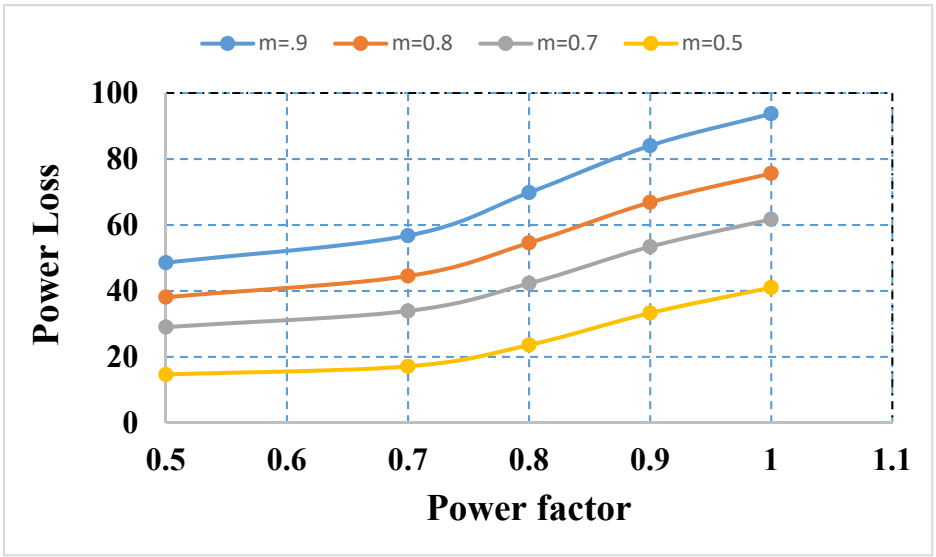
$$P_S = \sum_{k=1}^{9}\left(\sum_{m=1}^{N_{on}} P_{S,on,nm} + \sum_{m=1}^{N_{off}} P_{S,off,nm}\right)$$

4.2. Conduction Losses (P_C)

The losses due to the internal resistance of each semiconductor component are used to calculate the losses that occur due to them. Results are obtained for the resistive load by using the PLECS software. Figure 7a shows the efficiency versus power factor curve from which we observe that efficiency will be at a maximum when the modulation index equals one, and efficiency will decrease as the modulation index decreases. Figure 7b shows the power loss vs. power factor curve as we observe that power loss will be more for modulation index equals one and continues decreasing as we decrease the modulation index. Figure 7c shows the variation of THD with a change in the modulation.

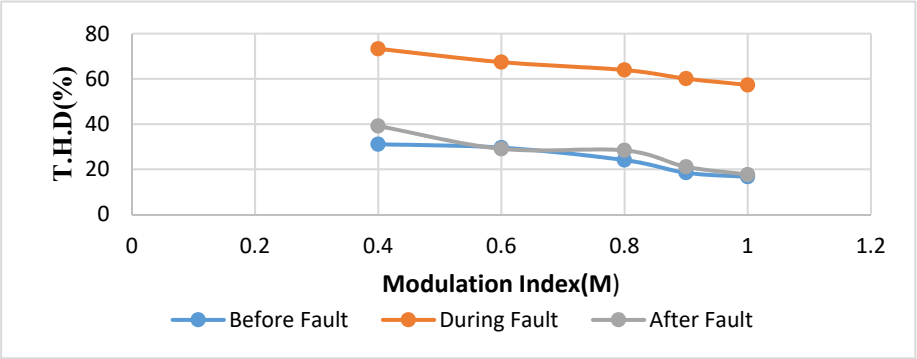


(**a**)



(**b**)

Figure 7. *Cont.*



(**c**)

Figure 7. (**a**) Modulation index vs. efficiency, (**b**) modulation index vs. power loss, and (**c**) modulation index vs. THD.

5. Simulation Results and Discussions

The Simulink model of the proposed five-level fault-tolerant topology was developed using Matlab2018a, and for verifying the simulation results obtained, experimental hardware results were also recorded.

Simulation Results

The output voltage, load current, and THD for the (RL) load during the normal condition are simulated in the modified FT-MLI, as well as the output voltage and load current for the fault in each switch. The simulation is carried out using MATLAB/Simulink. Table 4 lists all of the device parameters used in the simulation. The magnitude of the DC voltage sources for simulation purposes was considered to be 100 and 50 volts. The output voltage and current, as shown in Figure 8a, are obtained at Z = 100 Ω + 318 mH during the normal condition, and the number of output voltage levels was reduced to three, as shown in Figure 8b when the modulation index changed from 1 to 0.5. This shows that the number of voltage levels is dependent on the modulation index. The THD of the output voltage at 50Hz is 16.12%, which is shown in Figure 8c.

Table 4. Parameters used for simulation.

Parameters	Specification
DC Supply 1	100
DC Supply 2	50
Load Resistance and Inductance Value	R = 100 Ω, L = 318 mH
Modulation Index	1
Switching Frequency	50 HZ

The simulation results, as shown in Figure 9, are obtained when a fault in each switch of the proposed fault-tolerant topology occurs. In Figure 9, pre-fault, during-fault, and after-fault conditions have been shown. Pre-fault refers to the normal operation when no fault has occurred. During-fault refers to the system when the fault occurs to the circuit. Figure 9a shows the output waveform during the fault in switch S_1 in which the output voltage regains its level after the fault. Figure 9b shows the output waveform when the fault occurs in switch S_2, where the output voltage level reduces to three-level. Figure 9c shows the output waveform when there is a fault in switch S_3, reducing the output voltage to three-level. Figure 9d shows the output waveform due to a fault in switch S_4, which maintains the output voltage at five-level. Figure 9e shows the output waveform due to a fault in switch S_5, which maintains the output voltage at five-level. Figure 9f shows the output waveform due to a fault in switch S_6, which maintains the output voltage at five as the fault occurs. Figure 9g shows the output waveform due to a fault in switch S_7, which maintains the output voltage at five-level. Figure 9h shows the output waveform due to a fault in switch S_8, which maintains the output voltage at five-level. Figure 9i shows the output waveform due to a fault in Switch S_9, which maintains the output voltage at five-level.

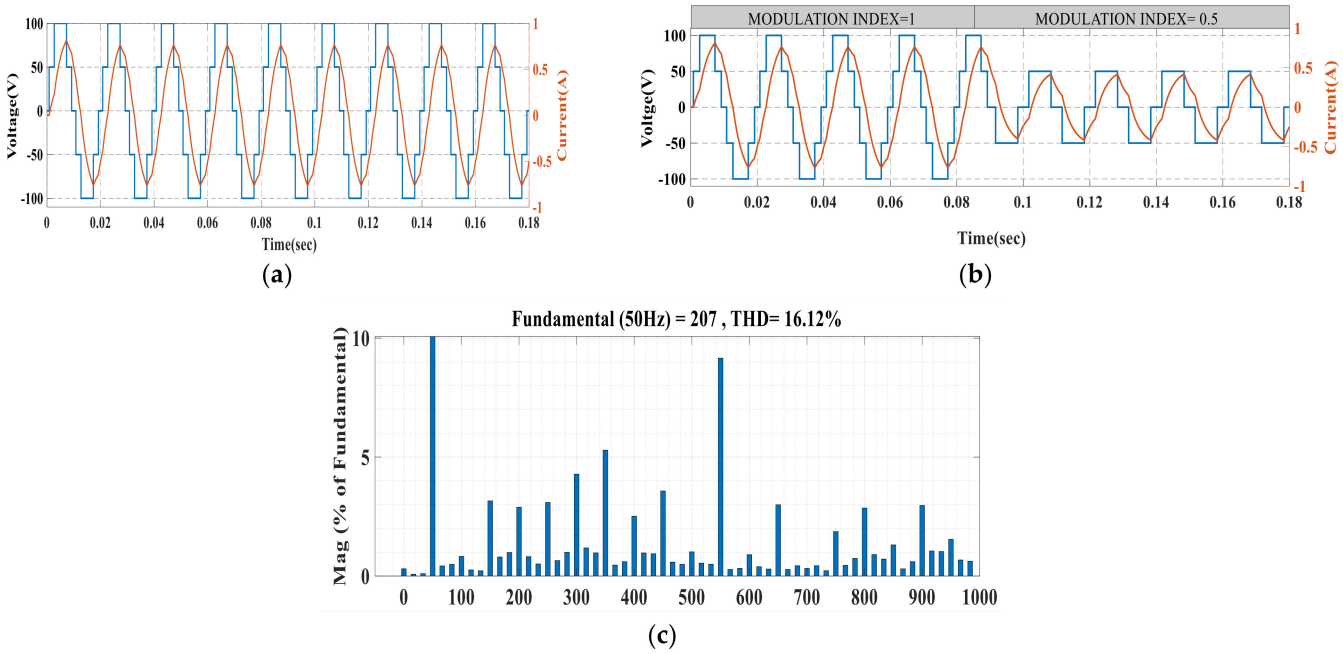


Figure 8. (**a**) Simulation results for output voltage and load current during normal condition, (**b**) output voltage and load current at modulation index 1 and 0.5, and (**c**) THD of voltage during normal conditioning.

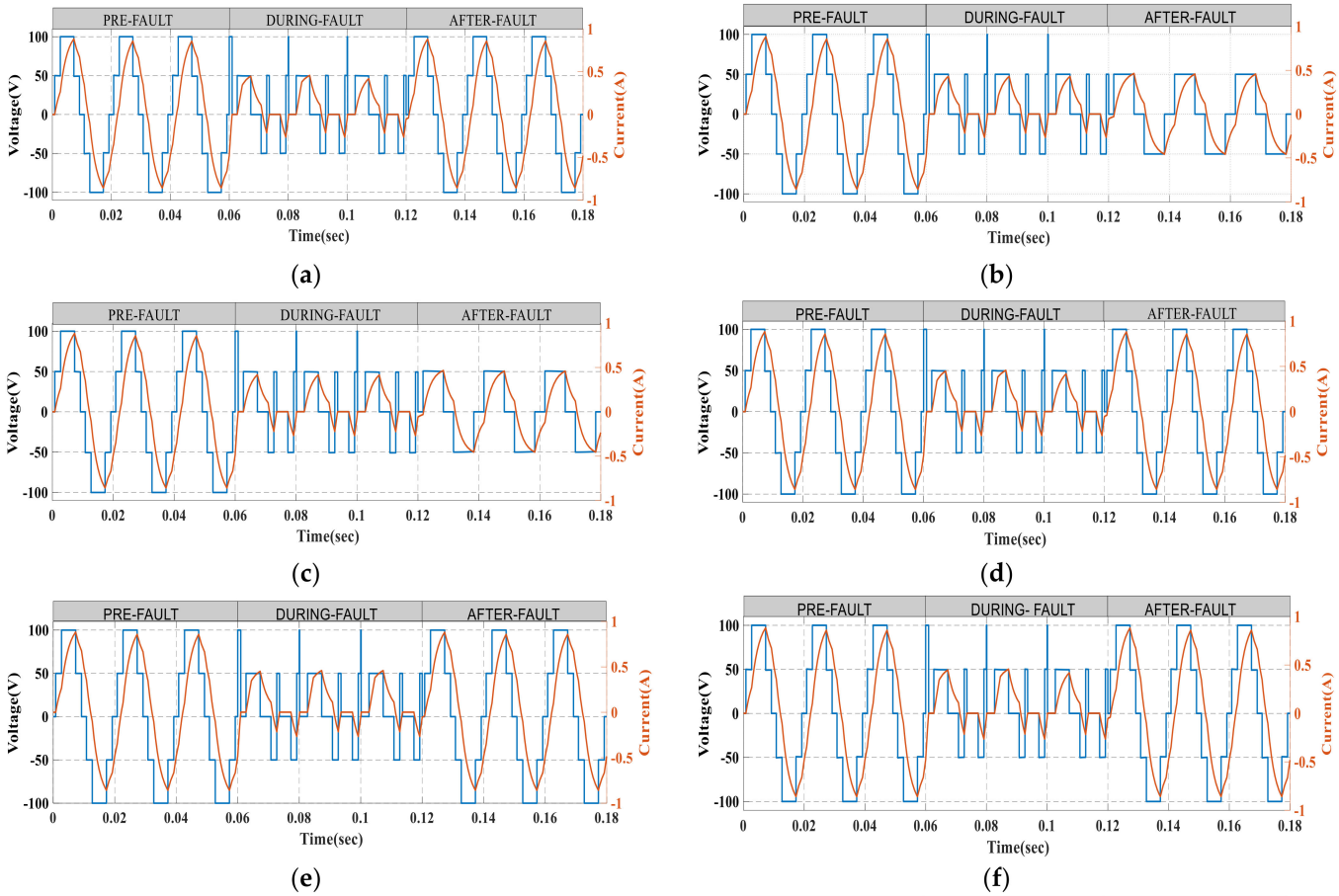


Figure 9. *Cont.*

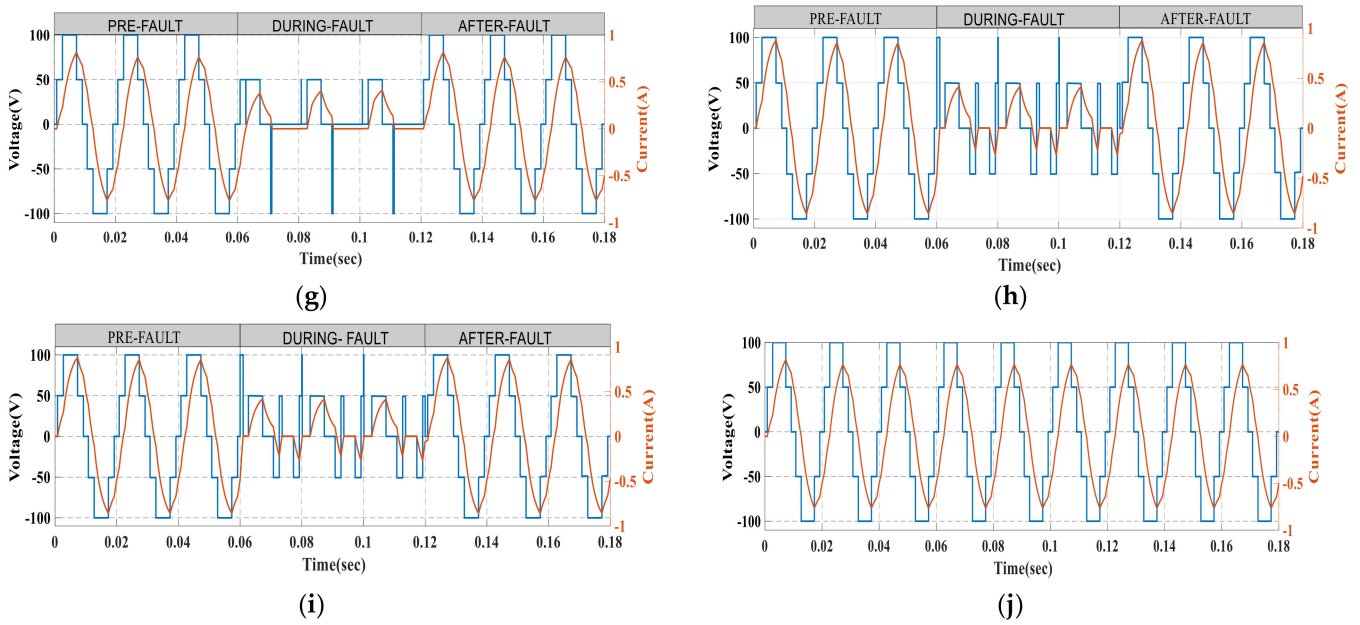


Figure 9. (**a**) Fault in Switch S_1/S_1 S_4, (**b**) fault in switch S_2, (**c**) fault in switch S_3, (**d**) fault in switch S_4, (**e**) fault in switch S_5, (**f**) fault in switch S_6, (**g**) fault in switch S_7/S_1 S_7, (**h**) fault in switch S_8/S_1 S_8, (**i**) fault in switch S_9/S_1 S_9, and (**j**) output of PUC5 result in normal condition.

6. Experimental Setup and Results

A hardware setup has been designed to test the feasibility and resilience of the proposed FT topology. An experimental model testing setup is shown in Figure 10. Through the gate driver TLP250 (F) and a DSP real-time controller that works as an interface with MATLAB/Simulink, control signals are provided to operate the IGBTs (IGBTFGA25N120) of discrete power switching modules. Two DC sources of 120 and 60 volts, respectively, are used in the hardware setup to obtain the result at a load of R = 300 Ω. Figure 11a shows the output voltage and current during normal conditions with a step size of 40 V and a peak output voltage of 80 Vrms. The output current shown in the figure has a peak-to-peak current of 10.2 A. Figure 11b shows the THD of the output voltage for five-level in which the fundamental THD is 19.7%. Only odd-order harmonics are produced. Even-order harmonics are absent. Figure 11c shows the THD of the output current when the output is five-level. The THD of the fundamental output current is 24.7%. Figure 11d shows the THD of the output voltage when the levels of the output voltage are reduced to three-level. The THD of the fundamental output voltage is 41.2%. Table 5 lists all of the device parameters used in the experiment.

Table 5. Parameters for experimental validation.

Parameters	Specification Type
DC Voltage Source 1	60
DC Voltage Source 2	30
Switches	IGBTFGA25N120
Resistive Load	300 Ω
DSP Kit	C2000, Texas
Optocoupler	TLP250(TOSHIBA)
Modulation Index(M)	1
Switching Frequency	50 HZ

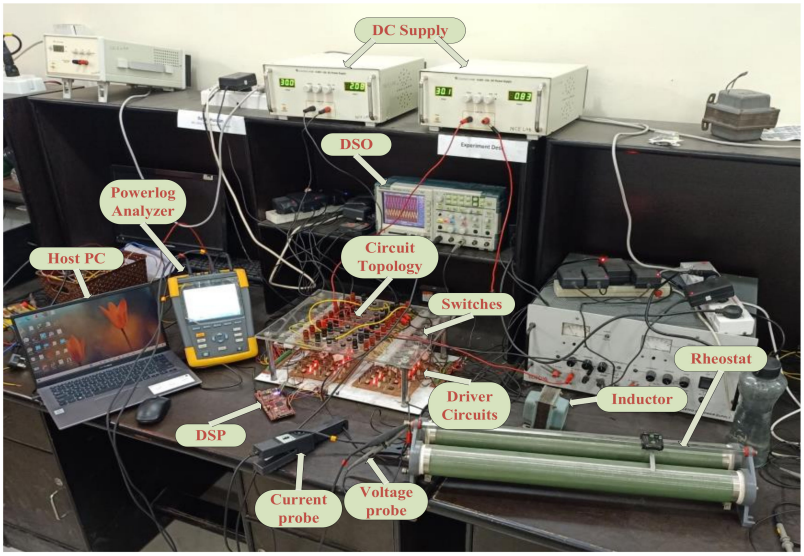


Figure 10. Hardware setup of the proposed topology.

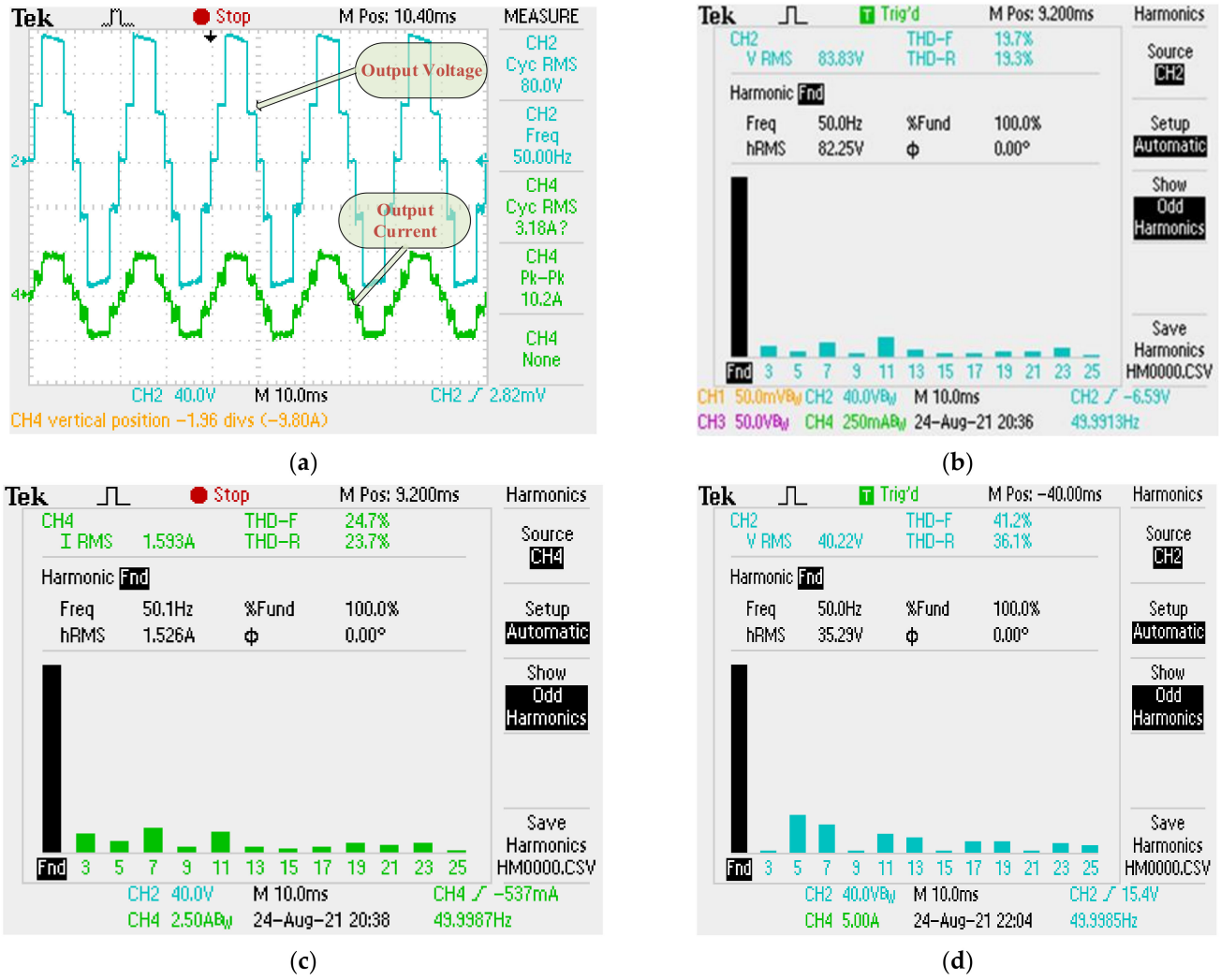


Figure 11. (**a**) Output voltage (V) and load current (A) during normal condition, (**b**) THD of output voltage for five-level, (**c**) THD of output current for five-level, and (**d**) THD of output voltage for three-level.

The output voltage and current waveforms during the fault condition, when the OC fault occurs at any switch, are shown in Figure 12. The output voltage and the output current are shown in Figure 12a when there is a fault in switch S_1. The voltage and current have an 80V (rms) peak and a 10.2 A peak-to-peak value, respectively. Figure 12b shows the output waveforms (voltage and current) when there is a fault in switch S_2. The output waveforms obtained are of three-level after a fault condition. Figure 12c shows the output waveforms when there is a fault in switch S_3. The output waveforms obtained are of three-level. Figure 12d shows the output waveforms when there is a fault in switch S_4. The output waveforms obtained are of five-level. Figure 12e shows the output waveforms when there is a fault in switch S_5. The output waveforms obtained are of five-level. Figure 12f shows the output waveforms due to a fault in S_6. The output waveforms obtained are of five-level. Figure 12g shows the output waveforms when there is a fault in switch S_7. The output waveforms obtained are of five-level. Figure 12h shows the output waveforms when there is a fault in switch S_8. Figure 12i shows the output waveforms when there is a fault in switch S_9.

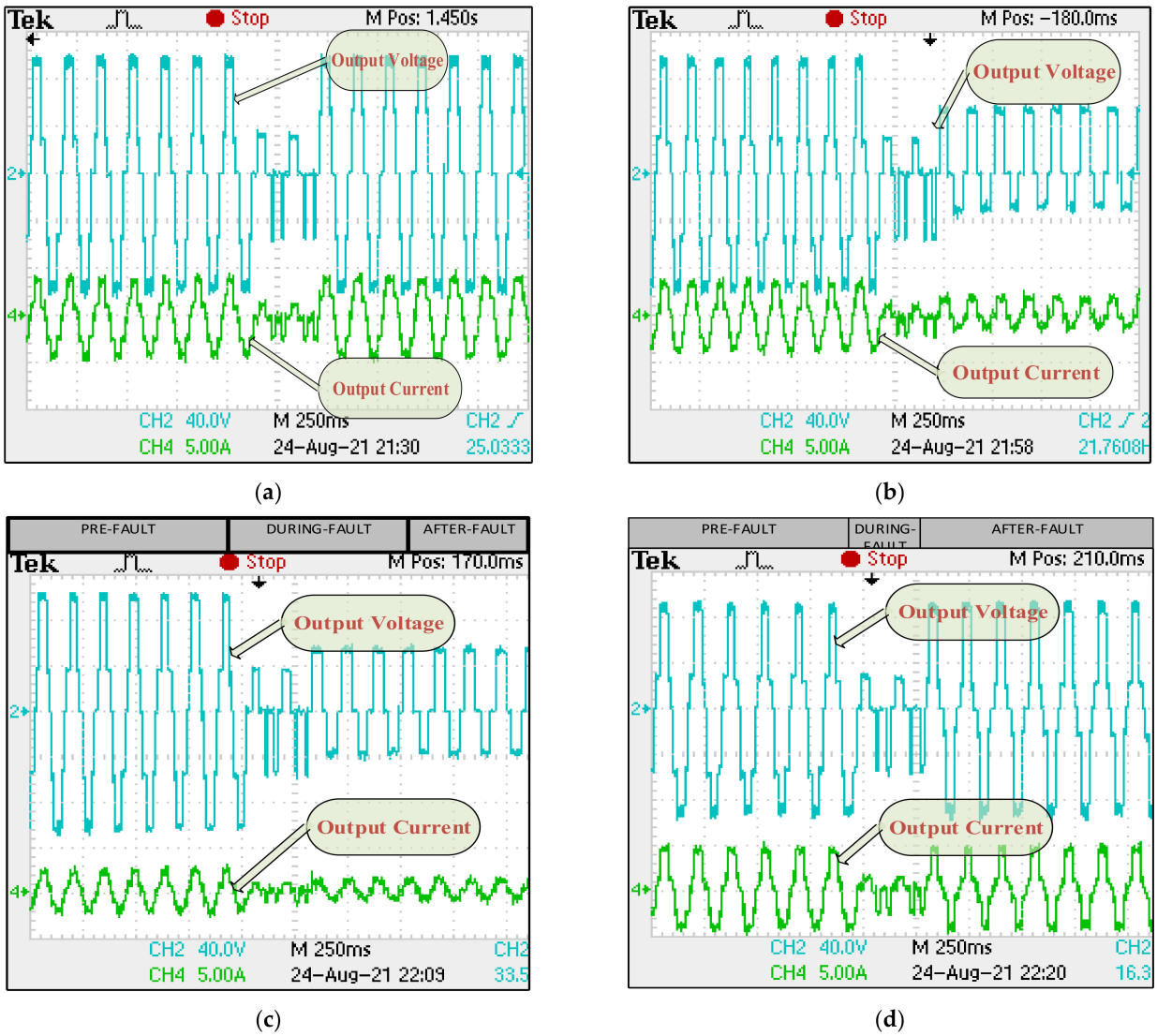


Figure 12. *Cont.*

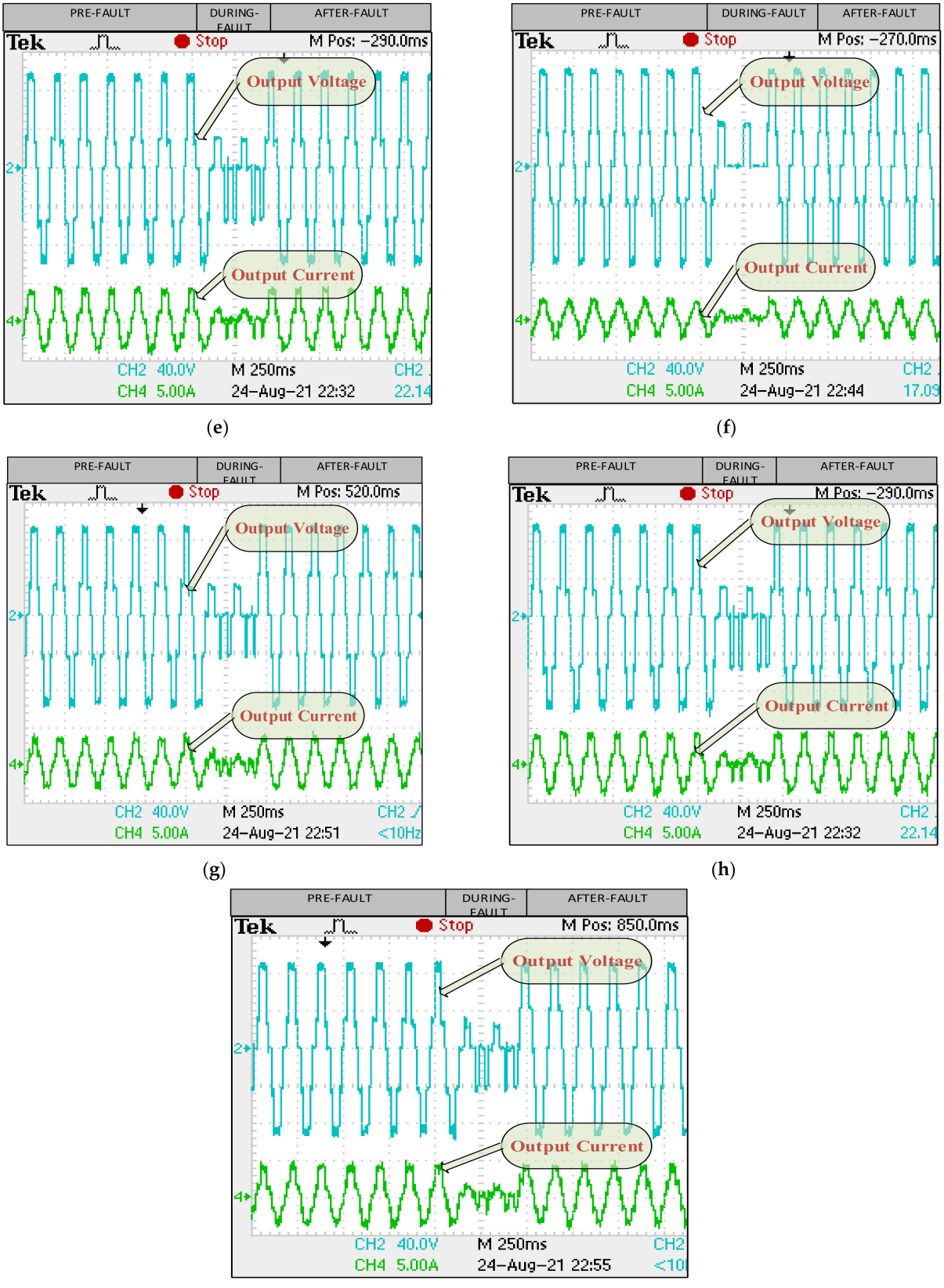


Figure 12. (**a**) Fault in switch S_1, (**b**) fault in switch S_2, (**c**) fault in switch S_3, (**d**) fault in switch S_4, (**e**) fault in switch S_5, (**f**) fault in switch S_6, (**g**) fault in switch S_7, (**h**) fault in switch S_8, and (**i**) fault in switch S_9.

7. Inverter Topologies Comparison

In Table 6, a comparison of the component count of single-phase five-level conventional topology has been made to the proposed fault-tolerant topology with respect to the DC source, capacitor, clamped diode, and active switches. Cascaded H-bridge inverters do not require a clamping diode or balancing capacitor, and their control complexity is low. Flying capacitors and neutral point diode-clamped MLIs have the disadvantage of requiring many capacitors and diodes to produce higher levels and very high control complexity. PUC5 does not require a clamping diode and has the advantage of a self-balancing capacitor with a low control complexity. Table 7 summarizes the different figures of merit considered for the comparative study with fault-tolerant topology. A comparison is made between the number of main switches, flying capacitors, DC bus capacitors, clamping diodes, and main diodes. The number of power switches plays a vital role in dictating the overall size and cost of the inverter. As the number of switches and other components increases, the overall cost, size, and complexity of the circuit also increase. A higher number of switches also increases the switching and conduction loss, which deteriorates the overall efficiency of the circuit. In Table 7, the proposed topology does not require a clamping diode, main diode, DC bus capacitor, additional auxiliary module, redundant leg, or impedance network, which reduces the circuit complexity and the total number of switches required, providing an advantage over the other published topologies. The cost factor (CF), which is used to compare the cost-per-level of the output voltage, is given as [14,15]. The CF for the proposed topology is comparable with PUC5 and the cascaded H-bridge, even though it has fault-tolerant capability and is far better than the other remaining topologies. In Figure 13, the simulation result of PUC5 demonstrates the depreciation in the output power quality when the topology is not fault-tolerant.

$$\text{Cost Factor} = \frac{(\text{No.of DC voltage source} + \text{Capacitor} + \text{Clamped Diode}) * \text{No.of Switches}}{\text{No.of output Voltage Level}}$$

Table 6. Comparison table for single-phase five-level.

Inverter Type	DC Sources	Capacitor	Clamped Diode	Active Switch	Total Parts Count	Control Com-plexity	Cost Factor
Cascaded-H Bridge	2	0	0	8	10	Low	3.2
NPC with Voltage Control	1	4	6	8	19	Very High	17.6
NPC without Voltage Control	4	0	6	8	18	Low	16
Flying Capacitor	1	3	0	6	10	High	4.8
PUC5	1	1	0	6	8	Very Low	2.4
Proposed Topology	2	0	0	9	11	Very Low	3.6

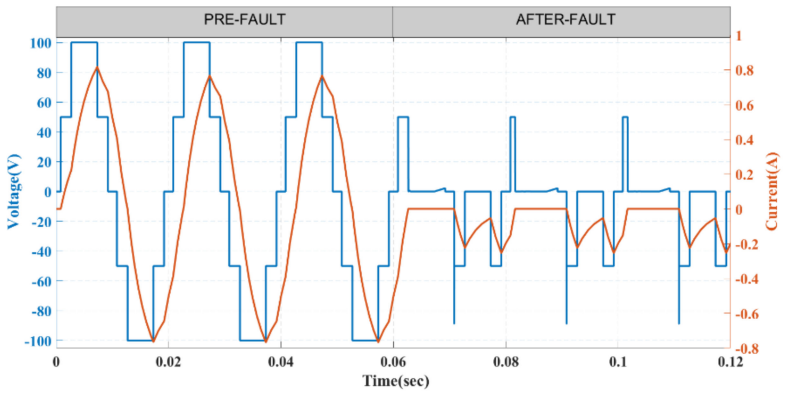


Figure 13. Pre-fault and post-fault output voltage and current waveform for PUC5.

Table 7. Comparison of the total parts count for the proposed fault-tolerant topology with the existing topology.

Inverter Configuration	[16]	[17]	[18]	[19]	[20]	Proposed Topology
Main Switches	14	16	12	18	12	9
Main Diodes	14	16	12	18	12	0
Clamping Diodes	4	0	0	0	0	0
DC Bus Capacitor	0	0	0	2	0	0
Flying Capacitor	0	0	0	1	0	0
Voltage Level in Healthy Condition	5	7	5	3	3	5
DC Voltage Sources	2	3	1	1	2	2
Cost Factor	56	43.42	31.2	138	56	3.6
Bi-directional Switches	0	0	0	0	0	0
Auxiliary Module	✘	✓	✘	✘	✘	✘
Redundant Leg	✓	✘	✓	✘	✓	✘
Impedance Network	✘	✘	✘	✓	✘	✘
SingleSwitch OCFaultTolerant	✓	✓	✓	✓	✓	✓

8. Conclusions

This paper proposed a modified five-level fault-tolerant topology. By strategically putting three power switches in the circuit, the changed topology is obtained from the existing (five-level) topology which results in redundant paths. These redundant pathways can still provide output in the event of power switch open-circuit faults, conferring fault-tolerant properties and making the architecture fully fault-tolerant. In addition, under healthy, faulty, and post-fault operation, the updated FT-MLI topologies have two DC sources, with the second DC source set at half the value of the first DC voltage source. The control scheme has been operated using the nearest level control technique. The working principle and its flexibility against open-circuit failures have been proven by simulation and experimental results. The simulation, coupled with the experimental data, confirmed the modified FT-MLI topology's feasibility and effectiveness. Furthermore, a comparison with recently published topologies shows the effectiveness of the proposed topology.

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