Reconfiguration of a Multilevel Inverter with Trapezoidal Pulse Width Modulation

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Abstract: This paper presents different multi-carrier unipolar trapezoidal pulse width modulation strategies for a reduced switch asymmetrical multilevel inverter. The different strategies are phase disposition, alternative phase opposition and disposition, and carrier overlapping and variable frequency that involve triangular waves as carriers with a unipolar trapezoidal wave as a reference. The reduced switch, asymmetrical multilevel inverter operation was examined for generating the seven-level output voltage using Matlab/Simulink 2009b and the results were verified with a real-time laboratory-based experimental setup using a field-programmable gate array. Different parameter analyses, such as total harmonic distortion, fundamental root mean square voltage, and distortion factor, were analyzed with different modulation indices to investigate the performance of the selected topology. Unipolar trapezoidal pulse width modulation provides a higher root mean square voltage value.

Keywords: multilevel inverter; multi-carrier pulse width modulation; FPGA; trapezoidal pulse width modulation; inverter

1. Introduction

The term multilevel originated from the two-level inverter. The elementary concept of the multilevel inverter (MLI) is used to achieve high power with several DC voltage sources. In an MLI, the amplitude of the output voltage is improved, which reduces the overall harmonic content and switching stress of the device [1,2]. Generally, the flying capacitor multilevel inverter (FCMLI), diode clamped multilevel inverter (DCMLI), and cascaded multilevel inverter (CHBMLI) are the three main topologies of the conventional multilevel inverter. The FCMLI is hard to comprehend because it contains many clamping capacitors and a DC bus capacitor. The DCMLI structure remains the same as the FCMLI, but clamping diodes are used instead of clamping capacitors. In addition, FCMLI and DCMLI are difficult to extend the level of the output voltage because of the use of the DC bus capacitor. The balancing of the DC bus capacitor is the major concern in both topologies [3,4]. The most popular conventional MLI is CHBMLI, which has many attractive features, such as a simple and modular design, requires fewer component counts, and averts a unbalance in capacitor voltage. The symmetric CHBMLI requires isolated DC sources with equal voltage whereas the asymmetric requires isolated

DC sources with unequal voltage. The DC source ratios 1:2:4 and 1:3:9 are termed as binary and trinary, respectively [5].

Subsequently, several reduced switch MLI topologies have been addressed in symmetric, asymmetric, and hybrid conditions with pros and cons for the different applications. In [6], a stepped ladder-type cascaded inverter was presented. The presented ladder-type converter circuit consists on series connection of unit cells and it's generated the maximum number of levels with fewer semiconductor devices, and supplied the sources and voltage on the switches. In [7], a lower switching frequency control pulse width modulation (PWM) technique was applied to MLI-fed AC drives. Lower switching frequency decreased the switching losses of the power semiconductor devices but increased the total harmonic distortion. In [8], a new topology for symmetric and asymmetric MLI was developed. An asymmetric MLI produced a high output voltage level compared to a symmetric MLI. A nine-level cascade neutral point clamped inverter with low switching frequency pulse width modulation (PWM) was presented in [9]. The capacitor voltage balancing was the major concern. Additional control techniques are required to maintain the capacitor voltage. A hybrid MLI based on a diode clamped type for both symmetrical and asymmetrical configurations was presented in [10]. However, the topology required more number of components. A different elementary division for CMLI was introduced in [11]. Each elementary division was connected in series, which produced only a positive level output voltage. An H-bridge was included with the elementary division to produce the output voltage in both positive and negative sequences. However, the basic unit required a greater component count. The harmonic investigation for a three-level NPCMLI-fed induction motor drive was investigated in [12]. In-phase sinusoidal PWM and phase opposition PWM were used to examine the system. The in-phase PWM method provided better results than the phase opposition. In addition, conventional PWM was used. An asymmetrical MLI for traction drives was discussed in [13]. A new hybrid inverter topology with common mode voltage elimination for an induction motor drive was presented in [14]. This topology has only one DC source and different voltage levels were generated using the floating capacitors. A reduced switch cascaded multilevel inverter with several transformers and a single DC source was discussed in [15]. A transformer on the secondary side was used to increase the output voltage level, but the cost and size of the transformer are very high. In [16], an effective structure of an MLI that increases the number of output voltage levels with a reduced number of circuit components was presented. This topology could not prefer a higher power application because it had the diodes with a combination of switches. A novel PWM modulating technique for a hybrid multilevel inverter was described in [17]. The carrier waveform originated from the phase disposition carrier arrangement. Novel carrier-based PWM in neutral-point (NP) balancing in the three-level inverter was presented in [18]. A hybrid modulation technique for cascaded MLI for high power applications in renewable energy systems was examined in [19]. A new dual port asymmetrical MLI with reduced conversion stages to improve the overall conversion efficiency of the system was discussed in [20]. The neutral point clamped type and T-type three-level cells were combined to build a dual port asymmetrical MLI. The developed topology provided better efficiency for various DC/AC power systems [21].

The conventional topology DCMLI requires 6 DC bus capacitors, 12 switches, and 24 clamping diodes while the FCMLI requires 6 DC bus capacitors, 12 switches, and 12 clamping capacitors to generate the seven-level output voltage. However, the selected reduced switch asymmetric multilevel inverter requires only eight switches to generate the same voltage. This paper focuses mainly on the different multi-carrier strategies with a unipolar trapezoidal reference. The different multi-carrier arrangements, such as phase disposition (PD), alternative phase opposition and disposition (APOD), carrier overlapping (CO), and variable frequency (VF) pulse width modulation strategies are involved for generating the seven-level output voltage. The carrier count of a unipolar method has been reduced by half compared to the conventional PWM method, which is the main advantage of this implementation. The reduced switch single-phase MLI was tested with the resistive and inductive (RL) load using the Matlab/Simulink (2009b). Experimental work was carried out using an FPGA system

for strengthening the simulation results. The different parameters were evaluated and compared with each other at different modulation indices. The VFPWM method indicates a better performance compared to the other methods. In addition, the topology can be easily integrated with an appropriate solar-based converter by replacing the separate DC sources to achieve good performance in the photovoltaic application.

2. Single-Phase Seven-Level Reduced Switch Asymmetrical Inverter

Generally, the number of semiconductor device requirement for the MLI configurations depends on the number of output voltage level. However, increasing the number of power semiconductor devices leads to an increase in the topology design complexity, cost, and control difficulty. An asymmetric multilevel inverter (AMLI) can be utilized to achieve a higher number of output levels with the minimum number of power semiconductor devices compared to symmetric MLIs [8]. Feeding the converters with unequal DC voltages (asymmetrical feeding) increases the number of levels generated at the output voltage without any supplemental complexity to the existing symmetric topology.

Figure 1 shows the single-phase asymmetric seven-level inverter configuration. The selected asymmetric inverter consists of sub-multilevel inverters (low-power cell) and H-bridge (high-power cell) inverter. Sub-multilevel inverters are connected in series to achieve the desired number of voltage levels. Each sub-multilevel inverter has its own DC source and two power devices. The first sub-multilevel inverter consists of one DC source (V_{DC}) and two switches designated as S_1 and S_2 whereas the switches S_3 and S_4 and voltage source ($2V_{DC}$) are placed in the second sub-multilevel inverter. Both sub-multilevel inverters are connected in series and generate the required output voltage level at positive polarity. To operate as an inverter, it is necessary to change the voltage polarity in every half cycle. For this purpose, an H-bridge inverter is added with the sub-multilevel inverters. It is important to note that the switches of the H-bridge must withstand the higher voltage. This should be considered in the design of the inverter. However, these switches are turned ON or OFF only one time during a fundamental cycle. Therefore, these switches would be high-voltage and low-frequency switches. The zero output voltage is obtained when the switches S_2 and S_3 are turned ON, and simultaneously the other voltage levels are generated by the proper switching between the switches. Table 1 shows the switching table for generating each output voltage level. The generalized formulas for generating the output voltage level, maximum step output voltage, and the required number of devices and DC source are discussed below.
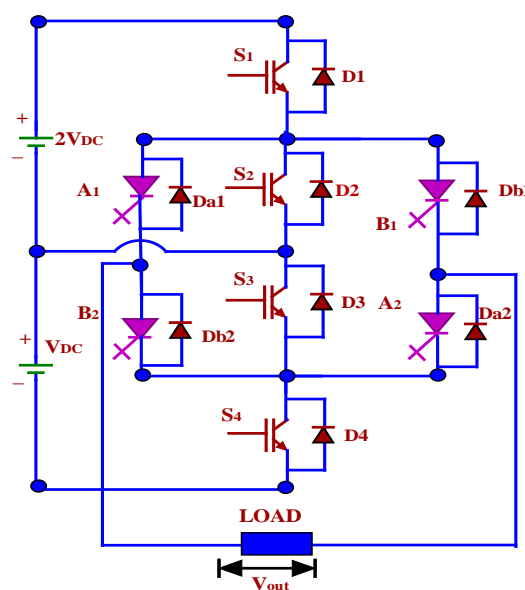

Figure 1. Single phase asymmetric seven-level inverter.

$$\text{Maximum step of output voltage } S_t = \left(2^j - 1\right) \text{Number of DC source } j = (1, 2, 3 \ldots n) \tag{1}$$

$$\text{Maximum level of output voltage } M = \left(2^{(j+1)} - 1\right) \tag{2}$$

$$\text{Maximum number of switches and driver circuit required} = 2j + 4 \tag{3}$$

$$\text{Magnitude of DC source } V_{dc,j} = \left(2^{(j-1)}\right) V_{dc} \tag{4}$$

$$\text{Magnitude of maximum output voltage } V_{out,max} = \left(2^j - 1\right) V_{dc} \text{ (or)} \tag{5}$$

$$V_{out,max} = (P - 1) V_{dc} \text{ where } P = 2^j \tag{6}$$

Table 1. Switching states for reduced switch multilevel inverter (MLI).

S_1	S_2	S_3	S_4	A_1	A_2	B_1	B_2	Output Level (V_{out})
1	0	0	1	1	1	0	0	$+3\,V_{dc}$
1	0	1	0	1	1	0	0	$+2\,V_{dc}$
0	1	0	1	1	1	0	0	$+1\,V_{dc}$
0	1	1	0	1	1	0	0	0
0	1	0	1	0	0	1	1	$-1\,V_{dc}$
1	0	1	0	0	0	1	1	$-2\,V_{dc}$
1	0	0	1	0	0	1	1	$-3\,V_{dc}$

3. Modulation Strategies for Asymmetrical Multilevel Inverters

MLIs offer several advantages, but the control strategies are quite challenging due to the complexity of generating the voltage level transition (or steps) [21]. Many PWM strategies are used in MLIs for different applications [22]. The PWM techniques are usually employed in MLIs, which can be classified into three main categories: (1) multi-step, fundamental frequency or staircase switching strategies, (2) space vector PWM strategies, and (3) carrier-based PWM strategies [23]. The first category needs pre-calculated switching angles for generating the PWM signals [23]. The space vector method will be very complicated for more than five output voltage levels due to increases in switching states [24]. The carrier-based PWM methods are simple to use when the number of output levels is more than five [25,26]. Therefore, the carrier-based PWM method is preferred in this work. The carrier-based PWM is categorized into three groups: (i) carrier disposition methods where the reference signal is sampled through the number of carrier signals displaced by increments of the reference amplitude, (ii) phase shift PWM methods where the multiple carriers are phase shifted accordingly, and (iii) a combination of carrier disposition and phase shift methods. Control freedom degree (CFD) exists to design the carriers in multi-carrier PWM strategies [27]. These strategies have more than one carrier option, which can be triangular, sawtooth, and some new function, etc. The modulating wave can be a sinusoidal or an advanced reference signal. The CFD technique is used to determine the carrier type and its frequency, amplitude, the phase of each carrier, and the offset between carriers. The multi-carrier PWM strategies can also be categorized into two types: multi-carrier bipolar PWM (MCBPWM) strategies and multi-carrier unipolar PWM (MCUPWM) strategies. In this work, the unipolar MCPWM strategy is selected for making quality output voltage. In the unipolar strategy, the reference wave may be a rectified reference wave or two reference waves with a 180-degree phase shift. The multi-carrier is positioned above the zero level. For the unipolar multi-carrier technique, the M-level inverter requires (M-1)/2 carriers with the same frequency f_c and same peak-to-peak amplitude A_c. The reference wave has the amplitude A_m and frequency f_m and it is placed at the zero reference. The different MCUPWM strategies, such as PDPWM, APODPWM, COPWM, and VFPWM, are utilized [8]. The carrier arrangement for the PDPWM strategy with

unipolar trapezoidal reference is shown in Figure 2. The carriers of the same frequency and same peak-to-peak amplitude are placed so that the bands they occupy are contiguous [28,29]. The carrier set is placed above the zero reference [28]. In the APODPWM strategy, the carriers of the same amplitude and same frequency are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees. Figure 3 shows the carrier arrangement for the APODPWM strategy [9]. The principle of COPWM is used to overlap the carriers with a single modulating signal. The carriers having the same frequency and same peak-to-peak amplitude are placed such that the bands they occupy overlap each other [8], as illustrated in Figure 4. In the VFPWM strategy, varying the carrier frequency based on the slope of the modulating wave in each band is represented in Figure 5. Positioned.
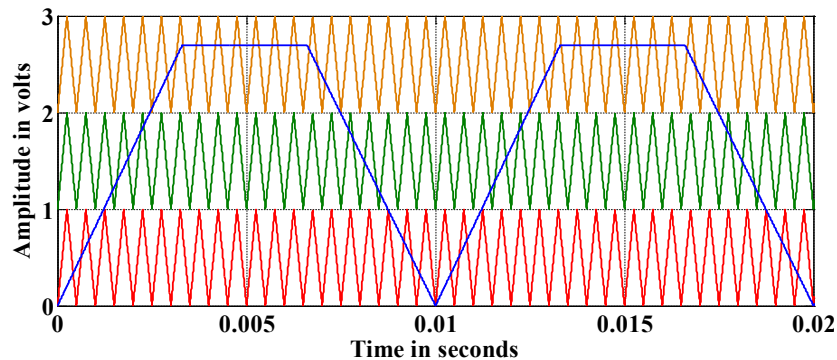
Figure 2. Carrier arrangement for the PDPWM strategy.
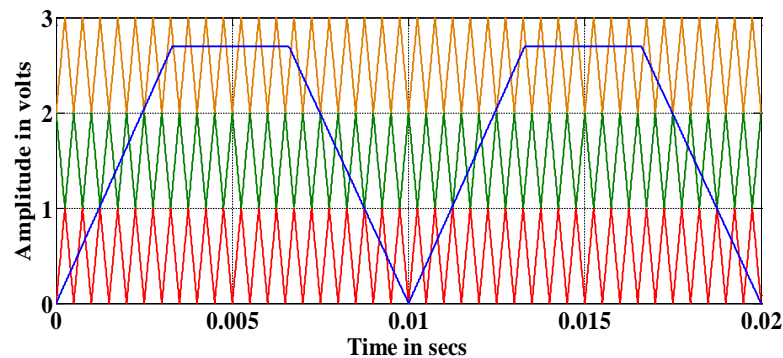
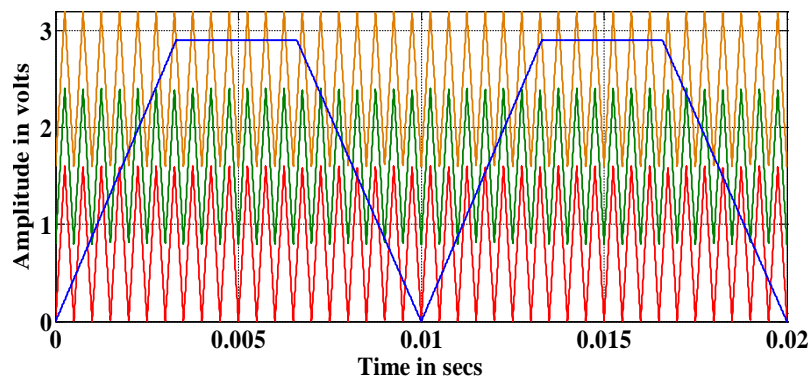**Figure 3.** Carrier arrangement for the APODPWM strategy.

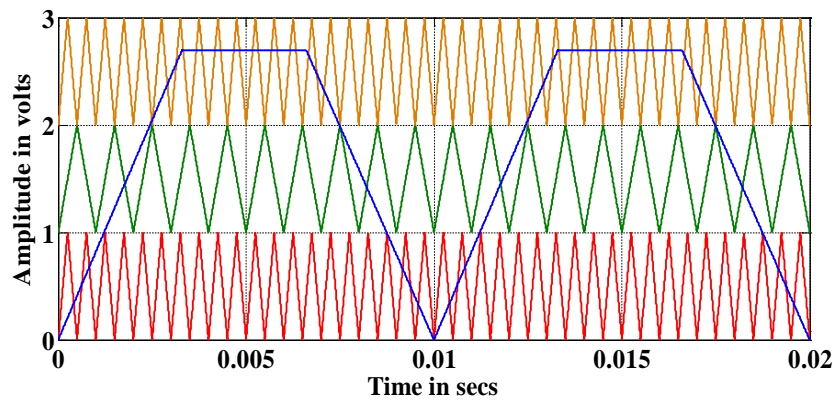**Figure 4.** Carrier arrangement for the COPWM strategy.

Figure 5. Carrier arrangement for the VFPWM strategy.

The main challenge is to reduce the switching losses of the inverter by reducing the switching frequency of the higher power cells. Therefore, instead of using MCUPWM (high-frequency carrier-based PWM) strategies in all the cells, the high-power cells are operated by a square waveform pattern switched at low frequency. Thus, the combination of MCUPWM (high frequency) and fundamental frequency (low frequency) switching modulation strategies was selected in this paper. In Figures 2–5, it is noticed that the three triangular carriers and a unipolar trapezoidal reference are used to generate the switching pulses. The unipolar trapezoidal wave is continuously compared with triangular carriers and generates the Boolean outputs. The outputs of each carrier are represented by Pw1 to Pw3. By using the logical expression with Boolean outputs based on a switching table, the required PWM pulses are generated for the respective switches to generate the desired output levels. The logical expression for all switches is given in Equation (7). The switches A_1 and A_2 are triggered on when the reference wave is greater than or equal to zero and B_1 and B_2 are triggered on when the reference wave is less than or equal to zero. Figure 6 shows the graphical representation for generating the switching pulses to get the desired output.

$$\left(\begin{array}{c} S_1 = Pw2 \\ S_2 = \overline{Pw2} \\ S_4 = \left[\overline{(Pw1 \oplus Pw2) \oplus Pw3} \right] \\ S_3 = \left[(Pw1 \oplus Pw2) \oplus Pw3 \right] \end{array} \right) \tag{7}$$
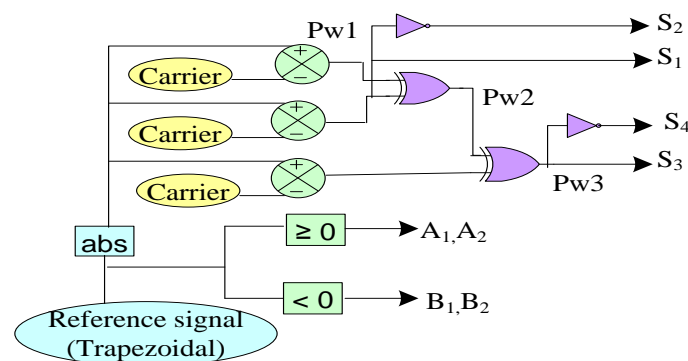

Figure 6. Logic circuits for pulse width modulation (PWM) generation.

4. Numerical Simulation Results

A single-phase reduced switch AMLI was modeled in Matlab/Simulink (2009a) to generate the seven-level output voltage by using a power system block set. Switching signals were developed using different multi-carrier unipolar PWM strategies as discussed in the previous section. Different parameters such as V_{dc1} = 6 V, V_{dc2} = 12 V, RL(load) = 100 Ω, 100 mH, f_c = 2000 Hz, and f_m = 50 Hz were utilized for simulation to evaluate the selected topology for the required output voltage. A simulation model was examined for different PWM strategies with various modulation indices ranging from 0.8–1. The % Total Harmonic Distortion (THD), fundamental root mean square (V_{RMS}) values, and % distortion factor (DF) for the output voltage with various modulation indices were measured and tabulated. Here, all the results are displayed with different PWM strategies at the modulation index of 0.9. Figure 7a–b shows the seven-level output voltage waveform and the current waveform generated by the PDPWM strategy and its fast Fourier transform (FFT) plot is shown in Figure 8. The value of %THD is 21.51%. Figure 9a–b shows the seven-level output voltage waveform and the current waveform generated by the APODPWM strategy and its FFT plot is shown in Figure 10. The value of %THD is 21.03%. Figure 11a–b shows the seven-level output voltage waveform and the current waveform generated by the COPWM strategy and its FFT plot is shown in Figure 12. The value of %THD is 25.63%. Figure 13a–b shows the seven-level output voltage waveform and the current waveform generated by the VFPWM strategy and its FFT plot is shown in Figure 14. The value of %THD is 20.06%.
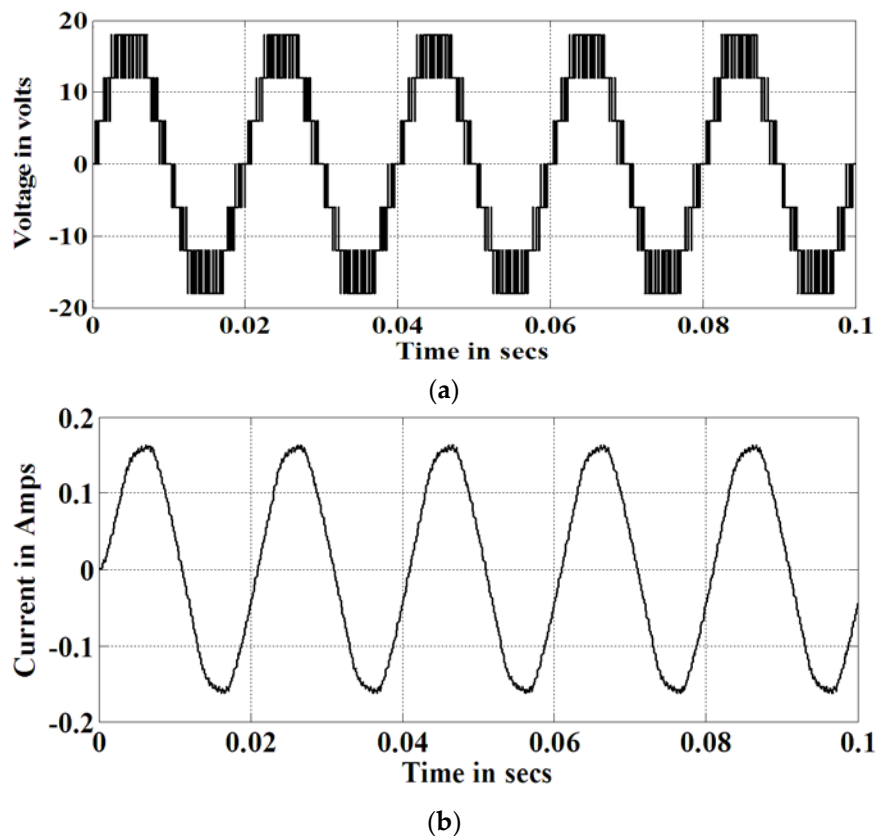

(a)

(b)

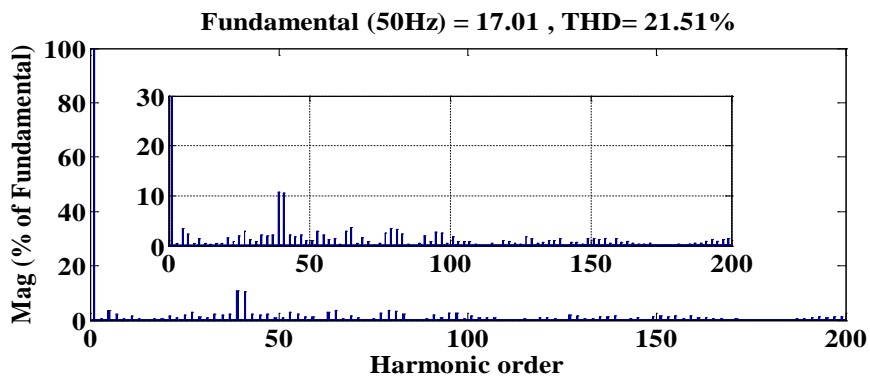**Figure 7.** Output waveform for the PDPWM strategy. (**a**) Voltage; (**b**) Current.

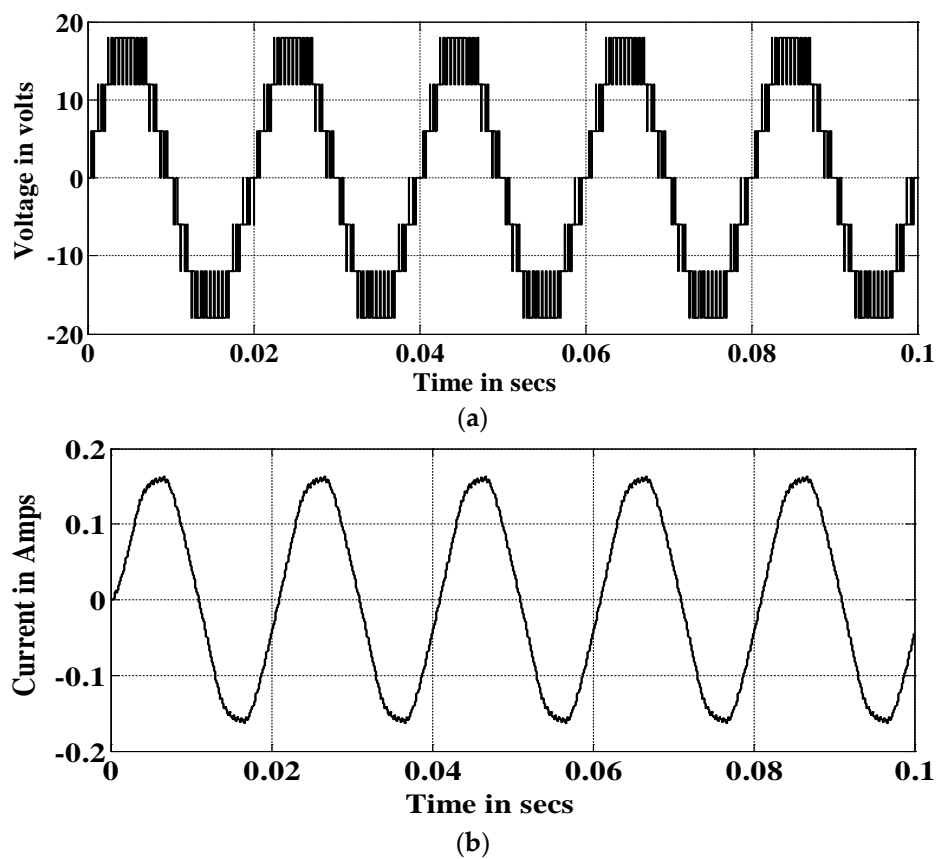**Figure 8.** Fast Fourier transform (FFT) plot for the output voltage of the PDPWM strategy.

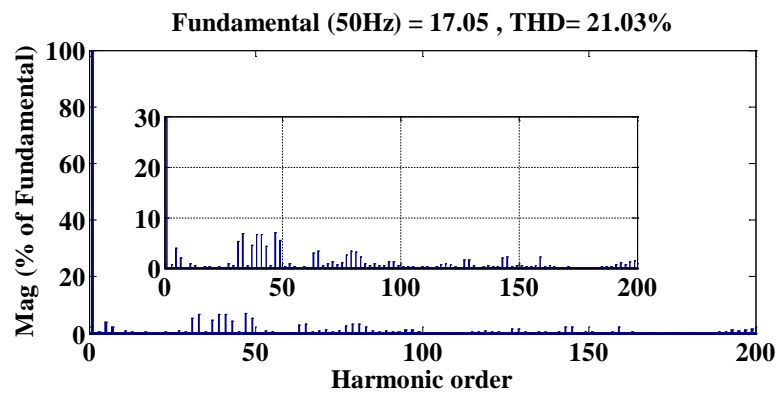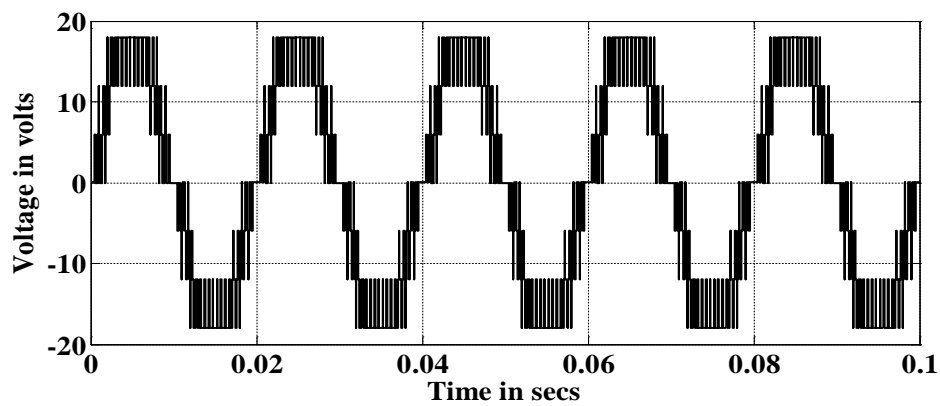**Figure 9.** Output waveform for the APODPWM strategy. (**a**) Voltage; (**b**) Current.
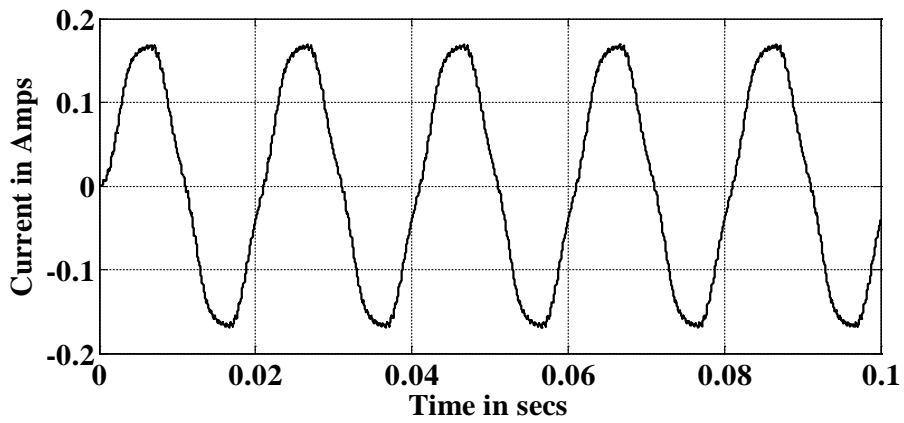
Figure 10. FFT plot for the output voltage of the APODPWM strategy.

(**a**)

(**b**)

Figure 11. Output waveform for the COPWM strategy. (**a**) Voltage; (**b**) Current.
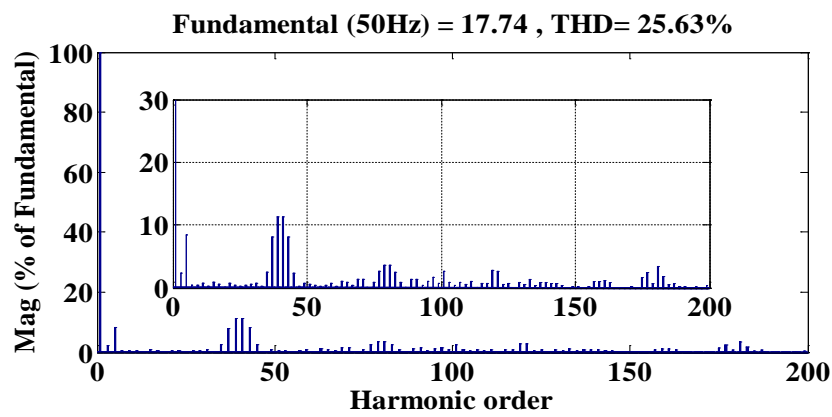
Figure 12. FFT plot for the output voltage of the COPWM strategy.

(**a**)

(**b**)

Figure 13. Output waveform for the VFPWM strategy. (**a**) Voltage; (**b**) Current.
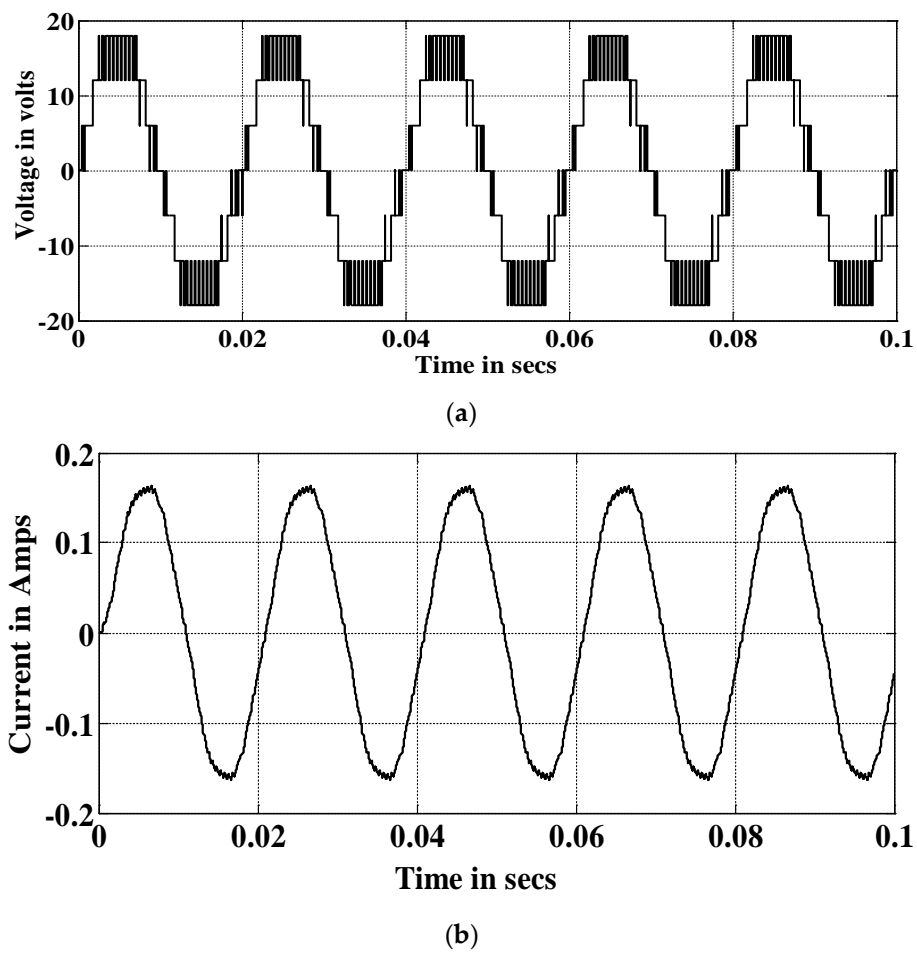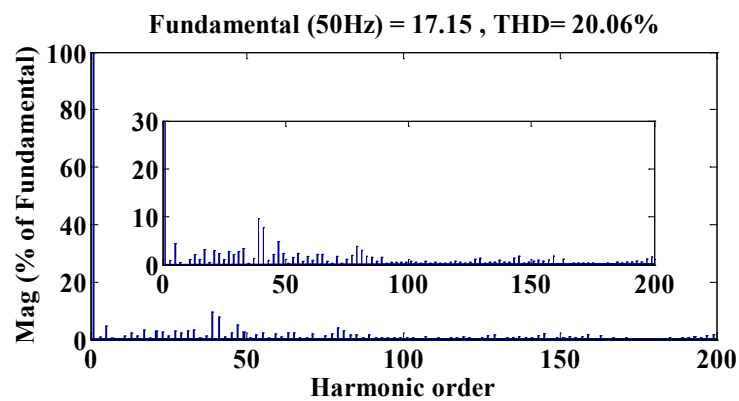
Figure 14. FFT plot for the output voltage of the VFPWM strategy.

Table 2. %THD for different modulation indices.

m_a	Simulation Results				Experimental Results			
	PD	APOD	CO	VF	PD	APOD	CO	VF
1	15.33	15.78	21.11	14.51	16.5	16.8	21.7	14.8
0.95	19.13	19.09	23.56	17.96	20.0	19.4	23.8	18.2
0.9	21.51	21.03	25.63	20.06	21.6	21.5	25.8	21.2
0.85	23.53	23.44	28.33	23.18	23.8	24	28.7	23.8
0.8	24.70	24.84	30.46	25.26	24.9	25.1	31	25.6

Table 3. V_{RMS} for different modulation indices.

m_a	Simulation Results				Experimental Results			
	PD	APOD	CO	VF	PD	APOD	CO	VF
1	12.734	12.8	13.54	13.36	13.1	13.0	13.7	13.5
0.95	12.72	12.72	13.03	12.75	12.9	12.8	13.2	12.8
0.9	12.03	12.06	12.54	12.13	12.1	12.3	12.9	12.4
0.85	11.37	11.36	11.88	11.42	11.7	11.6	12.0	11.8
0.8	10.72	10.69	11.32	10.71	10.9	10.8	11.5	10.9

Table 4. %Distortion factor for different modulation indices.

m_a	Simulation Results				Experimental Results			
	PD	APOD	CO	VF	PD	APOD	CO	VF
1	0.1798209	0.1747	0.3098	0.2333	0.181	0.183	0.291	0.272
0.95	0.1719129	0.1714	0.3401	0.2119	0.180	0.181	0.311	0.217
0.9	0.1564152	0.1716	0.4262	0.2092	0.160	0.178	0.399	0.210
0.85	0.1612577	0.1698	0.5707	0.1892	0.165	0.171	0.491	0.191
0.8	0.1783759	0.1681	0.7031	0.1539	0.181	0.170	0.575	0.165

The %THD comparison of the output voltage for different PWM switching strategies with various modulation indices is shown in Table 2 and the corresponding graphical representation is shown in Figure 15a. The %THD depends on the range of switching frequencies. The frequency modulation index m_f is defined as the ratio between the frequencies of the carrier f_{cr} and modulating wave f_m. When m_f is a small number (i.e., less than 21), its output spectrum contains low-frequency harmonics (sub-harmonics) causing high currents in transformers and inductors. Note that in the case of m_f being a large number, the amplitudes of the sub-harmonics are highly reduced and do not pose critical problems with the currents by inductors and transformers [6]. Therefore, the selected topology

generates low order harmonics with the obtained high frequency, but the order harmonic values have considerable limits, i.e., within the IEEE 519 standard. Hence, low order harmonics do not affect the system. From Figure 15a and Table 2, it is observed that the harmonic content of the output voltage is lower for the VFPWM strategy than the other strategies. The RMS comparison of the output voltage for different PWM switching strategies with various modulation indices is shown in Table 3 and the corresponding graphical representation is shown in Figure 15b. From Table 3 and Figure 15b, it is observed that the CO strategy provides the highest DC bus utilization compared with the other strategies. The %DF comparison of the output voltage for different PWM switching strategies with various modulation indices is shown in Table 4 and the corresponding graphical representation is shown in Figure 15c. It is further visualized from Table 4 and Figure 15c that the VFPWM strategy has relatively lower harmonics after second order attenuation, indicated by the %DF. Figure 15d shows the harmonic content (amplitude values) for individual harmonic order. From Figure 15d, it is noted that the lower and upper sidebands ($m_f \pm 1$ and $2m_f \pm 1$) appear in all strategies. In addition, the third-order harmonic is not dominant in all strategies. Harmonics corresponding to the center frequency m_f, $2m_f$ are minimum in all strategies. It is observed that the significant number of harmonics is avail by the VFPWM strategy using a trapezoidal reference carrier from the presented numerical results.
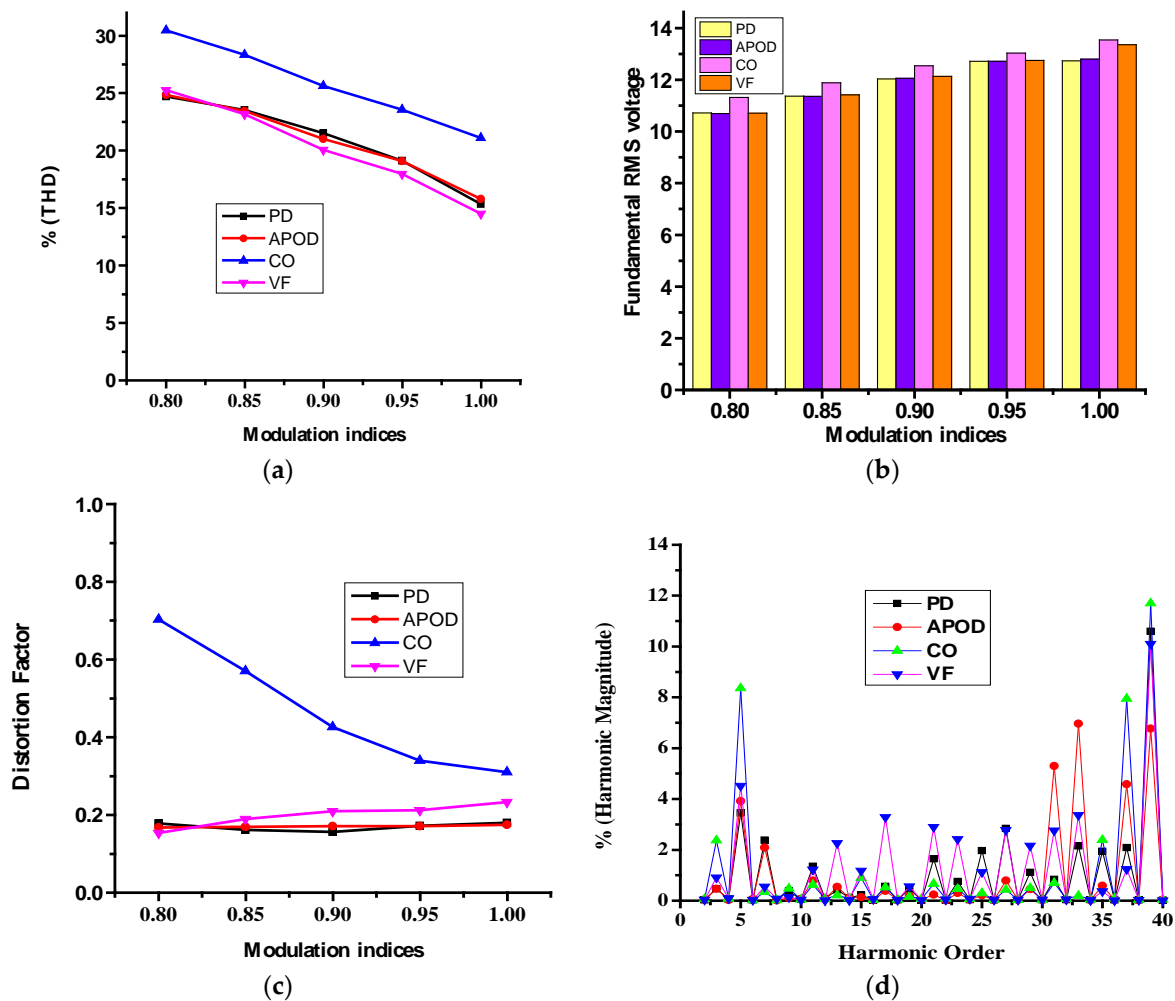

Figure 15. Different parameters for different modulation indices by simulation results: (**a**) %THD; (**b**) V_{RMS}; (**c**) %DF; (**d**) %Harmonic content for different harmonic orders.

5. Implementation of Reduced Switch AMLI Using FPGA for Experimental Results

This section describes the experimental results for reduced switch asymmetric multilevel to examine seven-level output voltage using the SPARTAN-3 FPGA system. FPGA was used for real-time implementation, which usually includes an on-chip PWM controller to reduce the complexity of PWM signal generation. Multi-carrier PWM strategies with a unipolar trapezoidal reference were used for generating the PWM signal to the selected topology. The simulation part was implemented in Matlab/Simulink (2009a) ((PWM signal generation)) and converted into an input signal of FPGA through the Xilinx software (compiled and converted into bits and then downloaded into FPGA for execution in the real-time process). Figure 16 depicts the laboratory-based experimental setup for reduced switch AMLI. The experimental setup consists of power converter module MLI and gate terminals are trigger through FPGA digital processor and is programme through Xilinx software. The hardware parameters includes the voltage value of the DC sources $V_{dc1} = 6$ V and $V_{dc2} = 12$ V, the RL load values are 100 Ω, 100 mH, and the switching carrier frequency (f_c) as 2000 Hz.
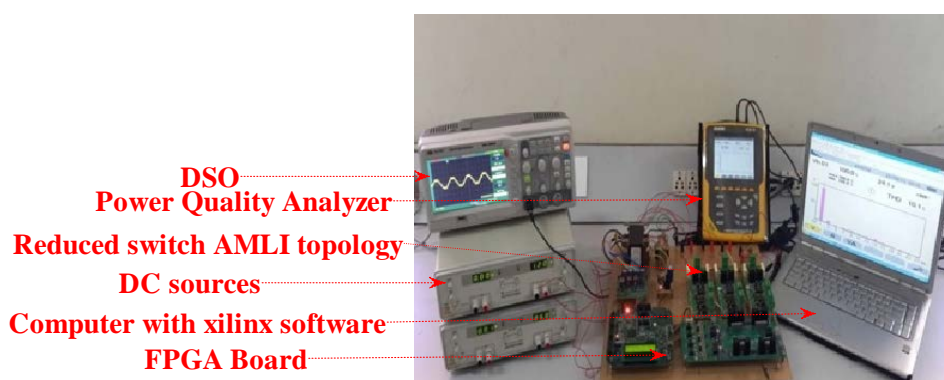

Figure 16. Laboratory-based experimental setup for asymmetric reduced switch multilevel inverter.

Figures 17–20 represent the experimental output voltage, output current waveform and its corresponding voltage FFT plot for PDPWM, APODPWM, COPWM, and VFPWM strategies. All output waveforms are portrayed for $m_a = 0.9$. From Figures 17a, 18a, 19a and 20a, it is observed that the peak-to-peak output voltage is 36 V, which is identical to the simulation results. An amplitude of each level is 6 V. From Figures 17b, 18b, 19b and 20b, it is evident that the experimental and simulation output currents are identical. The %THD values for different strategies are observed in Figures 17c, 18c, 19c and 20c. The value of %THD for PD, APOD, CO, and VF PWM are 21.6%, 21.5%, 25.8%, and 17.3%, respectively. Table 2 and Figure 21a show the comparison results of the %THD output voltage with various modulation indices for different PWM strategies. Table 3 and Figure 21b show the comparison results of the V_{RMS} output voltage with various modulation indices for different PWM strategies. Table 4 and Figure 21c show the comparison of the %DF output voltage with various modulation indices for different PWM strategies. From the results and comparison table, it is evident that the harmonic content of the output voltage is comparatively lower for the VFPWM strategy and the V_{RMS} output voltage for the COPWM strategy is higher than the other PWM strategies. In addition, from the results, the %DF is lower in the PDPWM strategy than the other PWM strategies.
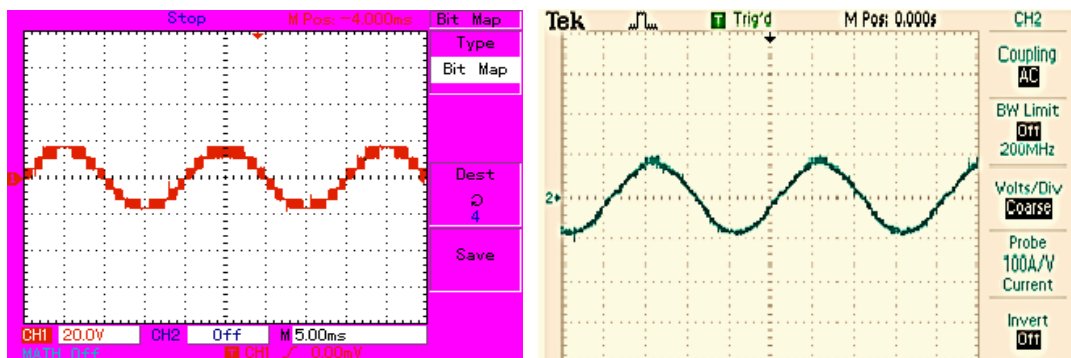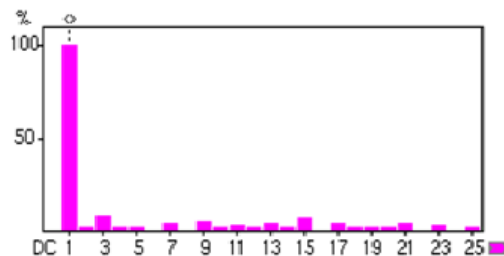
(a)　　　　　　　　　　　　　　　(b)
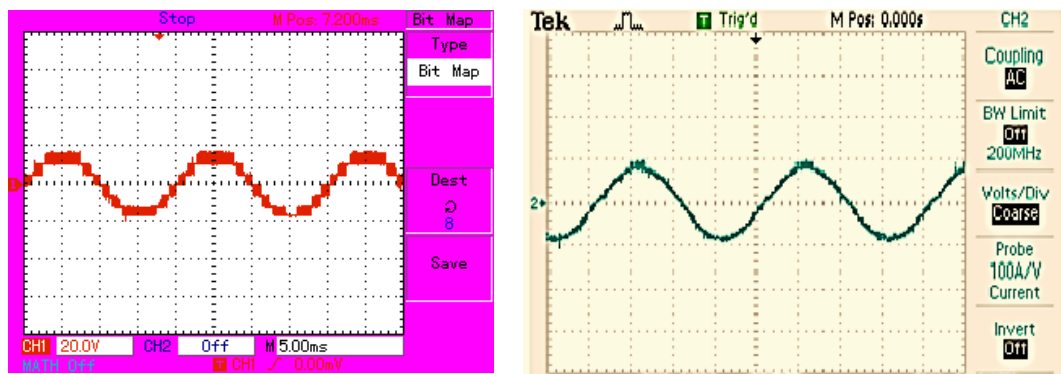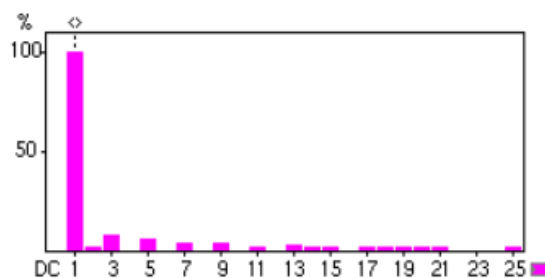
(c)

Figure 17. Experimental output waveform for the PDPWM strategy. (**a**) Voltage; (**b**) Current; (**c**) FFT plot for the output voltage.

(a)　　　　　　　　　　　　　　　(b)

(c)

Figure 18. Experimental output waveform for the APODPWM strategy. (**a**) Voltage; (**b**) Current; (**c**) FFT plot for the output voltage.

(a)

(b)

THD 25.6 %

(c)

Figure 19. Experimental output waveform for the COPWM strategy. (**a**) Voltage; (**b**) Current; (**c**) FFT plot for the output voltage.

(a)

(b)

THD 17.3 %

(c)

Figure 20. Experimental output waveform for the VFPWM strategy. (**a**) Voltage; (**b**) Current; (**c**) FFT plot for the output voltage.
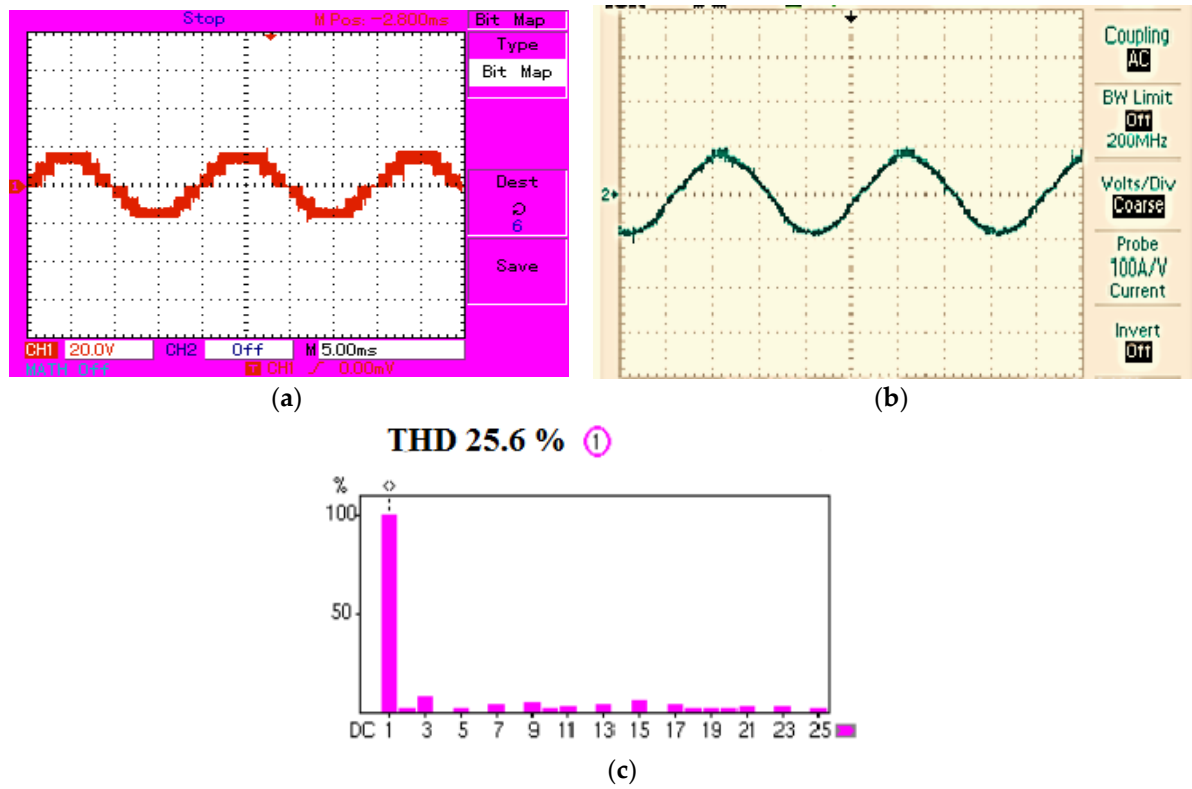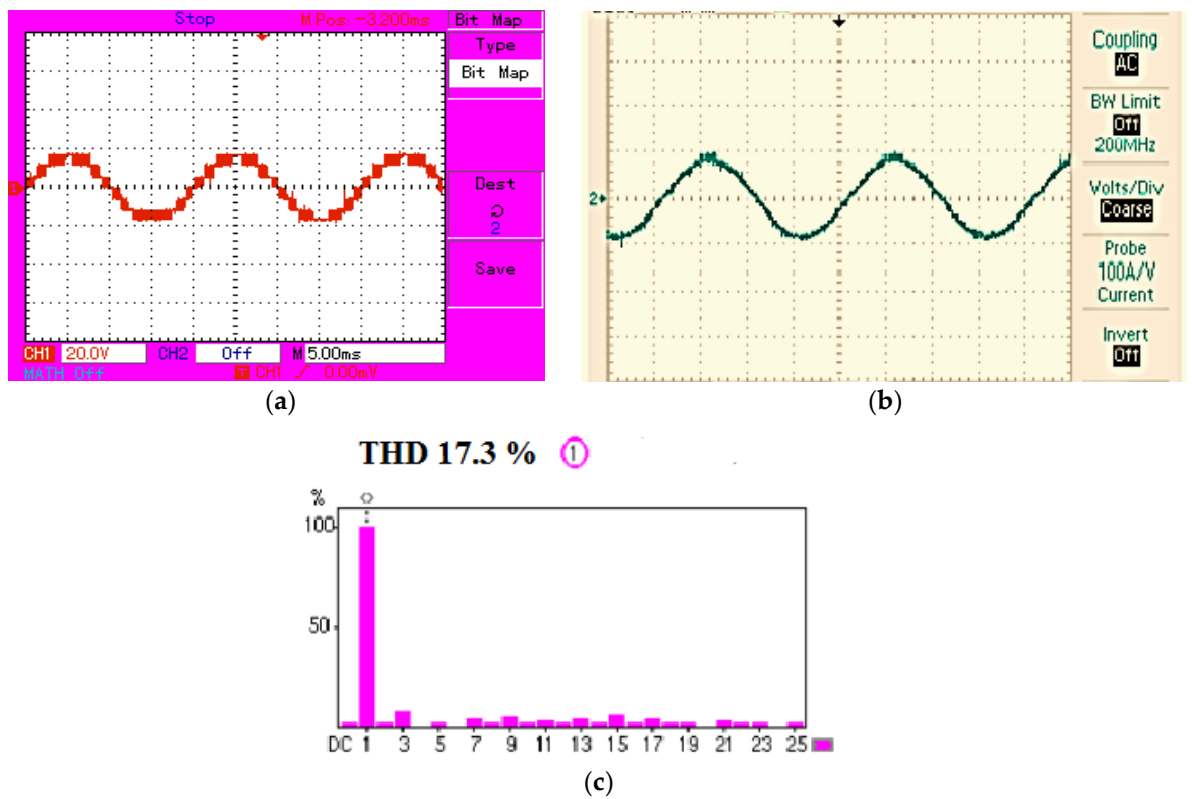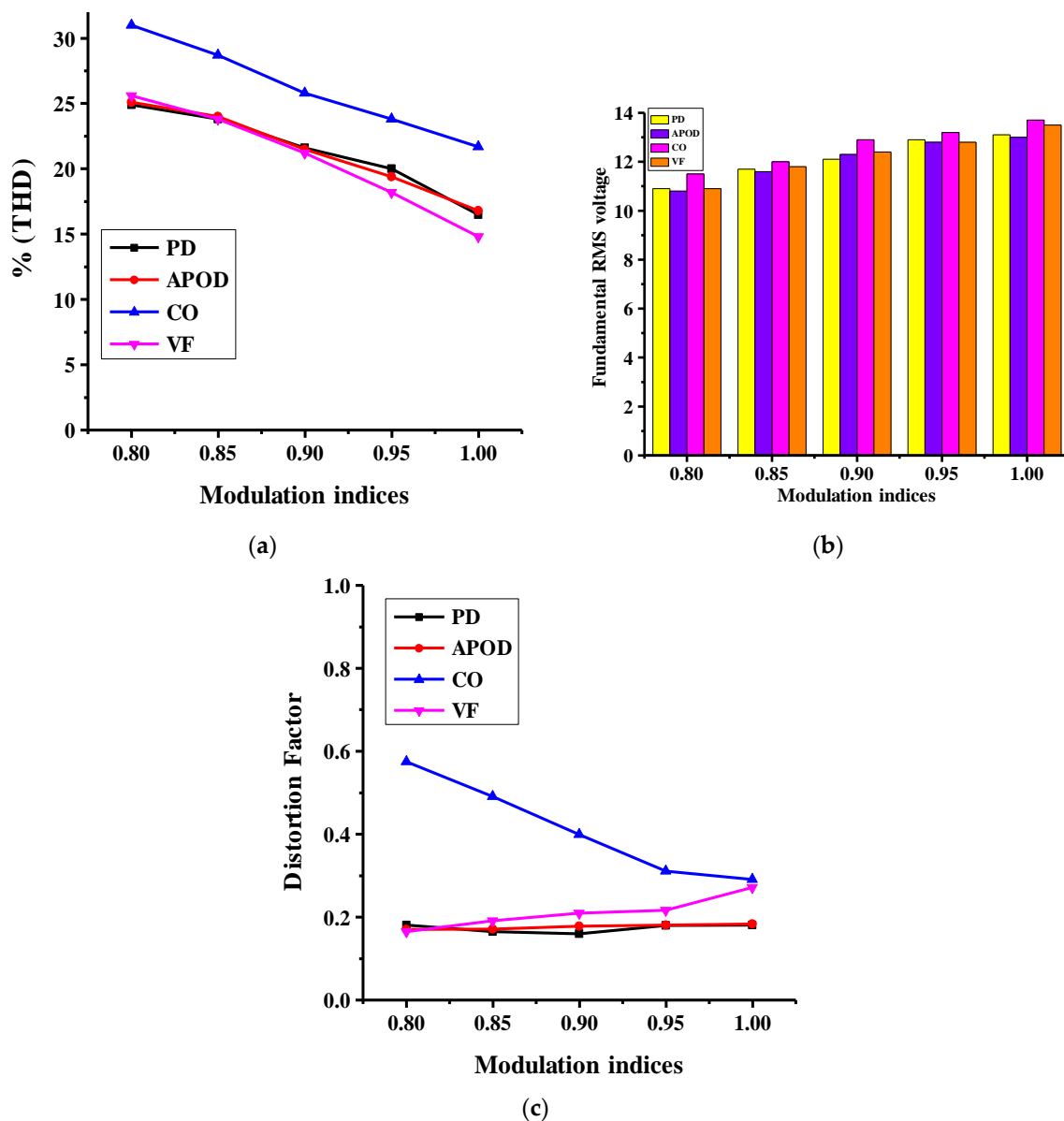
(**a**)

(**b**)

(**c**)

Figure 21. Different parameters for different modulation indices using experimental results: (**a**) %THD; (**b**) V_{RMS}; (**c**) %DF.

6. Conclusions

Asymmetric MLIs produce a higher output voltage level than symmetric MLIs. The selected reduced switch asymmetric MLI requires fewer components than conventional MLI topologies such as DCMLI and FCMLI. It requires only eight switches for generating the seven-level output voltage. The working principle of the selected topology and its mathematical expressions with respect to the maximum possible steps, the level of an output voltage, the magnitude value of the DC source, and the magnitude value of the maximum output voltage have been discussed. The sub-multilevel inverter of the reduced switch topology operated at a higher switching frequency whereas the H bridge operated at the fundamental switching frequency. The topology was examined with the different multi-carrier unipolar trapezoidal PWM strategies, such as PDPWM, APODPWM, COPWM, and VFPWM for generating the seven-level output voltage. By using the unipolar method, the carrier count was reduced by half compared with the conventional PWM method. The logic diagram for generating the switching pulses for the topology has been presented. The topology was examined with different

modulation index values from 0.8 to 1 for checking the potential of the reduced switch topology. It was designed using Matlab/Simulink (2009b) and implemented using the SPARTAN-3 FPGA system for the laboratory-based experimental results. Various performance parameters such as %THD, V_{RMS}, and %DF were evaluated for different strategies and compared with each other. From the results and discussion, it is evident that the VFPWM strategy produces less harmonic content than the other strategies. The COPWM strategy provides higher V_{RMS} than the other strategies. The simulation and experimental results were found to be satisfactory.

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