

Article

Hybrid Multicarrier Random Space Vector PWM for the Mitigation of Acoustic Noise

P. Madasamy ¹, Rajesh Verma ², C. Bharatiraja ^{3,*}, Barnabas Paul Glady J. ⁴, T. Srihari ⁵,
Josiah Lange Munda ⁶ and Lucian Mihet-Popa ^{7,*}

- ¹ Department of Electrical and Electronics Engineering, Alagappa Chettiar Government College Engineering and Technology, Karaikudi 630003, India; mjasmitha0612@gmail.com
- ² Department of Electrical Engineering, King Khalid University, Abha 62529, Saudi Arabia; rkishor@kku.edu.sa
- ³ Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Chennai 603203, India
- ⁴ Department of Electrical and Electronics Engineering, Sathyabama Institute of Science and Technology, Chennai 600119, India; barnabaspaulglady.eee@sathyabama.ac.in
- ⁵ Department of Electrical and Electronics Engineering, KSR Institute for Engineering Technology, KSR Kalvi Nagar, Tiruchengode 637215, India; k.t.srihari@gmail.com
- ⁶ Department of Electrical Engineering, Tshwane University of Technology, Pretoria 0001, South Africa; MundaJL@tut.ac.za
- ⁷ Faculty of Engineering, Østfold University College, Kobblerstredet 5, 1671 Kråkeroy-Fredrikstad, Norway
- * Correspondence: bharatiraja@gmail.com (C.B.); lucian.mihet@hiof.no (L.M.-P.)



check for updates

Citation: Madasamy, P.; Verma, R.; Bharatiraja, C.; J., B.P.G.; Srihari, T.; Munda, J.L.; Mihet-Popa, L. Hybrid Multicarrier Random Space Vector PWM for the Mitigation of Acoustic Noise. *Electronics* **2021**, *10*, 1483.

<https://doi.org/10.3390/electronics10121483>

Academic Editor: Flavio Canavero

Received: 16 February 2021

Accepted: 11 June 2021

Published: 19 June 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

Abstract: The pulse width modulation (PWM) inverter is an obvious choice for any industrial and power sector application. Particularly, industrial drives benefit from the higher DC-link utilization, acoustic noise, and vibration industrial standards. Many PWM techniques have been proposed to meet the drives' demand for higher DC-link utilization and lower harmonics suppression and noise reductions. Still, random PWM (RPWM) is the best candidate for reducing the acoustic noises. Few RPWM (RPWM) methods have been developed and investigated for the AC drive's PWM inverter. However, due to the lower randomness of the multiple frequency harmonics spectrum, reducing the drive noise is still challenging. These PWMs dealt with the spreading harmonics, thereby decreasing the harmonic effects on the system. However, these techniques are unsuccessful at maintaining the higher DC-link utilizations. Existing RPWM methods have less randomness and need complex digital circuitry. Therefore, this paper mainly deals with a combined RPWM principle in space vector PWM (SVPWM) to generate random PWM generation using an asymmetric frequency multicarrier called multicarrier random space vector PWM (MCRSVPWM). The SVPWM switching vectors with different frequency carrier are chosen with the aid of a random bi-nary bit generator. The proposed MCRSVPWM generates the pulses with a randomized triangular carrier (1 to 4 kHz), while the conventional RPWM method contains a random pulse position with a fixed frequency triangular carrier. The proposed PWM is capable of eradicating the high-frequency unpleasant acoustic noise more effectually than conventional RPWM with a shorter random frequency range. The simulation study is performed through MATLAB/Simulink for a 2 kW asynchronous induction motor drive. Experimental validation of the proposed MCRSVPWM is tested with a 2 kW six-switch (Power MOSFET-SCH2080KE) inverter power module-fed induction motor drive.

Keywords: pulse width modulation; random PWM; space vector PWM; voltage source PWM inverter; acoustic noise

1. Introduction

Pulse width modulated-based voltage source inverters (VSIs) are an unavoidable segment of industrial drive systems. These VSIs are needed in order to provide several advantages such as harmonics elimination, DC link utilization, common mode voltage

elimination, bearing current reduction, and acoustic noise reduction. Numerous forms of PWM schemes have been proposed in VSI to meet out the above requirements [1–3]. However, some of the PWM techniques are not helpful for acoustic noise reductions, which is essential to address for VSI-based drives [4–6]. Acoustic noise reduction is possible by spreading the harmonics throughout the harmonics spectrum [7]. For any PWM, the DC-link utilization is an additional criterion. Hence, the power electronics research using the random carrier PWM, which is called RPWM. In this PWM, unlike sine PWM (SPWM), random carriers are compared with the sinusoidal signal for arriving at the pulse [8].

The interest in developing PWM techniques for VSI-fed AC drives has increased in the current era due to their participation in industrial applications. The new age of space vector PWM (SVPWM) has been developed for induction motor drives with reduced common mode voltage and high utilization of DC-link voltage [9,10]. Several attempts have been proposed for the reduction of the AC drives' external noise suppression using PWM and filters [11–16]. However, the suppression filters reduce the noise by a considerable volume. These types of methods have led to broad claims for their use in electric-vehicle drive applications. However, they also involve higher cost regarding the drive installation and running.

The RPWM is the more promising of the two methods, as it helps to avoid whistling and electromagnetic interference (EMI) noises. RPWM is the best PWM to handle the induction motor drive with simple digital circuits and low cost, which leads to it being one of the most optimal PWM schemes [17]. The RPWM is realized by randomly changing the slope of the carrier wave. Generally, the prevailing RPWM can be grouped into three types: (1) random carrier frequency pulse width modulation (RCFPWM) [18], (2) random switching (RSPWM) [19] and (3) random pulse position pulse width modulation (RPPPWM) [20]. The RCFPWM is the most popular scheme, which dealt with randomly changing the switching events in an operating frequency cycle with the modulated carrier frequency. Here, the modification is made by changing the slope of the carrier triangular or the angle of the space vector reference. In RSPWM, instead of carrier triangular wave form change, the random signal is used to create a switching control gesture. Lin et al. implemented the RPWM using a simple digital hardware circuit, which is using only logic gates. In this paper, the authors generated the inverter gate pulses through the dedicated logical circuit, which dealt with the pseudorandom binary sequence (PRBS) bits [21]. As the carrier of the RPPPWM is using only a digital circuit, a fixed frequency triangular carrier signal or a saw-tooth carrier signal is used. Wang et al. [22] proposed a chaotic PWM method to decrease the EMI in electric drive systems. It enables the circuit to choose its own required carrier frequency. The paper also analyzed the effects of low-order noises and mechanical resonance. The RCF-PWM is more effective compared to the FCF-RPWM method [23,24]; meanwhile, the motor current spectrum is used to spread discrete components. In most of the practical real-time drive applications, the controller algorithm is coordinated with the inverter switching. Hence, the adjustable switching frequency disturbs the drive performance when it plays in the closed-loop systems [25,26]. In an electric drive system without exciting mechanical resonance, the fixed quasi-random carrier frequency PWM technique is proposed to abolish acoustical noise [12]. A random center distribution (RCD) problem is solved by the two-phase double zero-vector random center distribution structure. The modulation index of RCD is high and not reduced properly [25–27]. A fixed and randomized PWM technique for the fully controlled converter reduces the harmonic intensity, contributing efficiency [28,29]. The asymmetric carrier wave is implemented digitally, without employing external circuits [30–34]. More distinct states are essential to get random bit number generations. This process involves higher numbers of sequential digital circuits. Therefore, random bit number generations need higher circuit cost and implementation burden. Hence, the researchers recommended a linear feedback shift register (LFSR) for getting more randomness [35–39]. LFSR is commonly referred to as a pseudo-PWM code generator and works using a digital logical process of a binary number [29]. The length of the LFSR along with the clock frequency

present influences the amount of repetition. The sinusoidal reference is compared with the winning triangle carrier cycle in order to get the gating pulses. Still, various random PWM methods have been developed and investigated for the PWM inverter-fed drive noise reductions; still, the shortcomings of these method items include their lower randomness and complex digital circuitry.

Some of the PWM methods dealt with the spreading harmonics by decreasing the harmonic effects on the system. However, these techniques overlook the effect of acoustic noise and inverter DC-link utilizations. Therefore, this paper mainly deals with a combined RPWM principle in space vector PWM to generate random PWM generation. The SVPWM agreements with the multicarrier (different fixed frequencies as carrier waves) are chosen with the aid of a random binary bit generator. The proposed RSVM generated pulses with a randomized triangular carrier (1 kHz to 4 kHz), while the conventional RPWM method contains a random pulse position with a fixed frequency triangular carrier. The proposed PWM is capable of eradicating the high-frequency unpleasant acoustic noise more effectually than conventional RPWM with a shorter random frequency range.

The Field Programmable Gate Array (FPGA)-based two PRBS bit (8 bit and 16 bit) generators are used to generate the random binary. The SVPWM was developed using the same FPGA controller, and it is getting random carriers from a PRBS binary selector block. The simulation study is performed through MATLAB/Simulink software tool (2016.b) for a three-phase VSI connected 2 kW, 400 V, 2.5 A asynchronous induction motor drive. The experimental validation of the proposed RSVM is tested with a 2 kW six switch (Power MOSFET-SCH2080KE) inverter power module-fed induction motor drive. The simulation and hardware results show that the VSI and motor had comparable performance to the conventional MCRSVPWM; nevertheless, the noise power spectra of the current, voltage, dominant harmonic components, and acoustic noise spectra were reduced as compared with the reported RPWM methods.

This paper is structured as follows: Section 2 reviews the random pulse width modulation operating principles. In Section 3, the proposed Multicarrier Random Space Vector PWM is presented and analyzed. Sections 4 and 5 present the simulation and experimental results, respectively. Section 6 concludes the paper.

2. Review of Random Pulse Width Modulation

The important variance between standard PWM and random PWM methods is that the pulse width signal is no longer restricted to a few fundamental frequencies. The control relies on switching frequency (carrier frequency) and the modulated signal.

The following section explains the RPWM generation for six switch voltage source inverters. The VSI is shown in Figure 1, where three legs and six switches are used to synthesize three-phase AC power. The VSI should generate the symmetry-less THD voltage and current. The reduction of THD is possible for spreading the harmonics spectra. Figure 2 shows the RPWM pulse arrangement. Here, the random carrier is achieved through a digital binary assignment process PRBS. In general, the RPWM processes triangular carrier waves (fixed frequency carrier), and multiplexer and shift register are used in the random carrier. Figure 2 shows the conventional pseudorandom binary sequence RPWM.

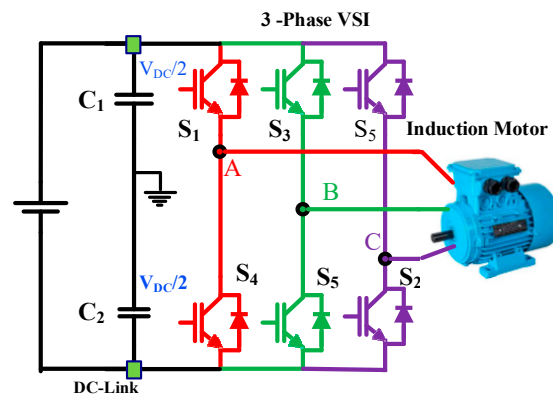


Figure 1. Three-phase VSI-fed inductor control.

Figure 2 shows that the fixed frequency triangular carrier ‘C’ is given through multiplexer (MUX) in ‘C’ and ‘C-’ sequence.

Fixed Frequency Triangle Wave

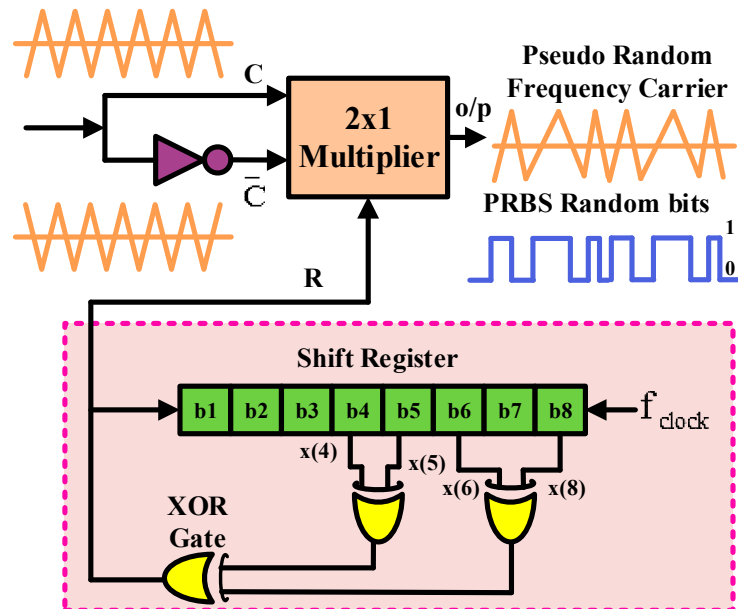


Figure 2. Conventional pseudorandom binary sequence RPWM.

Here, the ‘C-’ is the opposite phase of ‘C’ derived using ‘NOT’ gate. The ‘C’ and ‘C-’ are randomly chosen, and the triangular carrier waves with fixed frequency “C-” with an opposite phase of “C” are given by the selected signal (P) of the multiplexer. The multiplexer is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal. The MUX obtains the selected signal through the pseudorandom binary sequence shift register. The PRBS shift register is normally an 8/16 bit register, including the Exclusive OR (XOR) gate. Based on the values of the particular bit, the PRBS gives random binary logic.

In Figure 3, the ‘2 × 1’ multiplexer selects ‘C’, where ‘P’ is ‘1’. Similarly, when ‘P’ is ‘1’, then ‘C-’ is selected. The reported pseudorandom frequency used two triangular waveforms with the same frequency to synthesize the proposed random carrier. Therefore, the randomness is limited. Hence, the proposed random carrier technique uses the multiple randomness by using different frequency carriers.

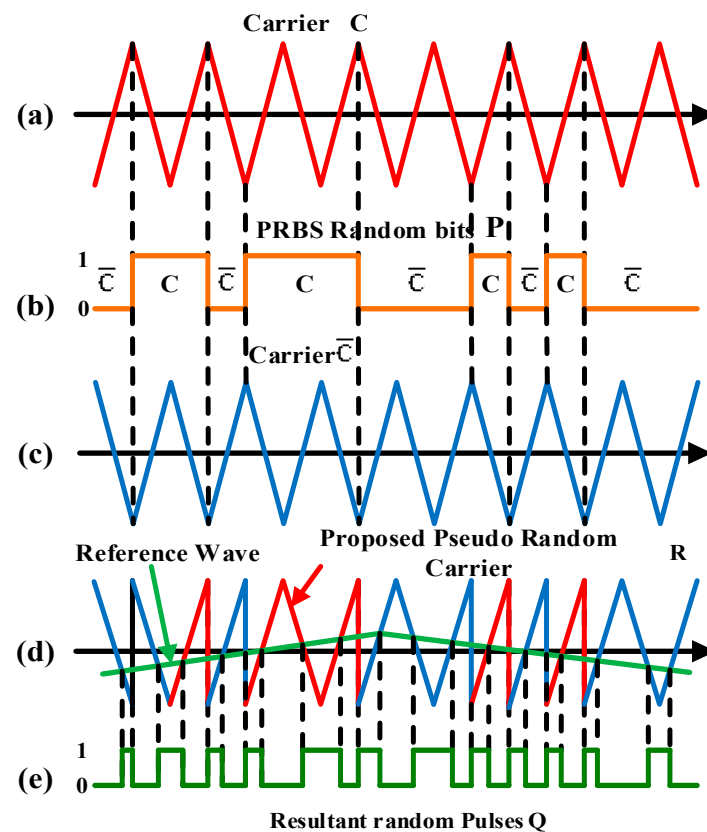


Figure 3. RPWM pulse arrangement. (a). Carrier signal and reference signals, (b). PRBS random bit, (c) Inverted Carrier signal and reference signal, (d). Mixed multi frequency carrier and reference signal, (e). Resultant random pulses.

3. Proposed Multicarrier Random Space Vector PWM

The RCPWM practice is basically related to conventional SPWM, the only variance being the usage of two different triangular carriers, which are the prerequisite frequency and 180-degree phase shifting on the carrier. RPWM targets the way of overwhelming the voltage and a current harmonic, which reduces the current ripple and torque ripple. For improving the inverter DC-link consumption performance, the RPWM is connected with SVPWM, which improves the SVPWM and RPWM quality on the VSI-connected drive. The proposed PWM generates the multiple carriers with a random pattern, and it is applied to SVD to generate the switching timings. The offered multicarrier random space vector PWM structure is presented in Figure 4.

The four carrier signals with different frequencies of 1 kHz, 2 kHz, 3 kHz, and 4 kHz (random values) are made to generate the randomness carrier. In order to merge these random carrier signals, four 3×1 multiplexers (MUX) are used, and finally, the MUX output is given to the 4×1 multiplexer. The 8-bit PRBS as well as 16-bit PRBS generator are used to generate random '0' and '1' sequence, which manipulate the random combination of four different carrier frequency signals. The randomness is present in the output in the sense that one element value in a sequence is not dependent on any other element sequence. Each carrier signal is selected through MUX and random binary sequence.

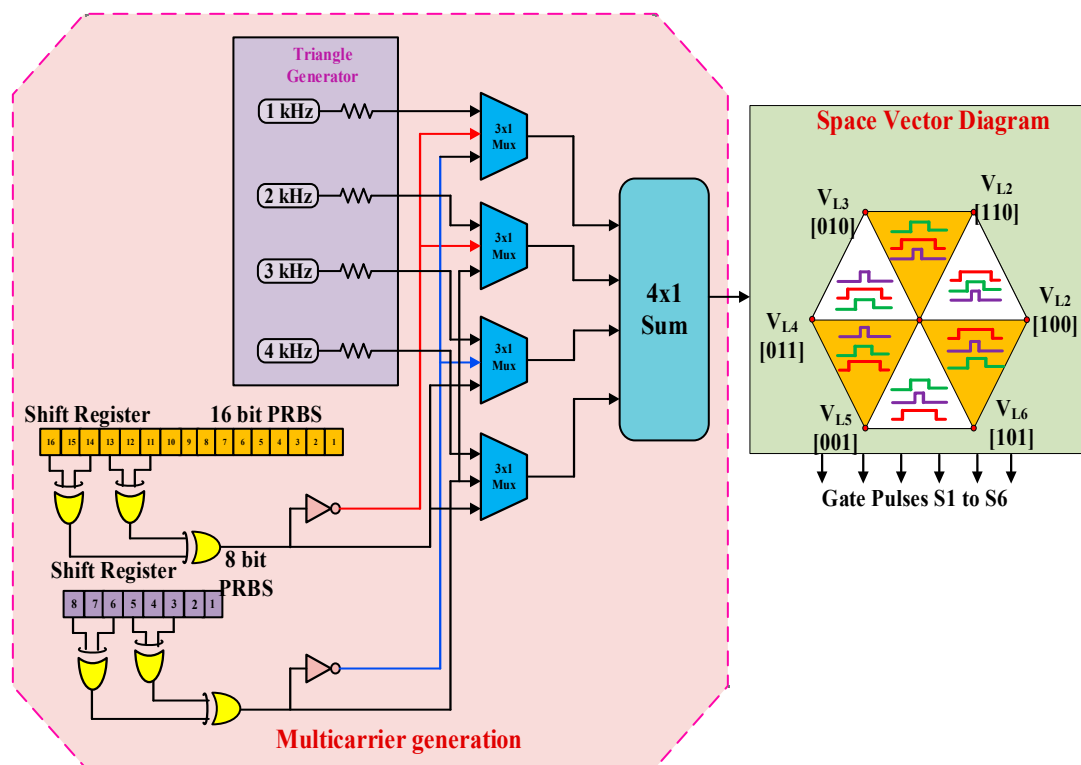


Figure 4. Proposed MCRSVPWM scheme.

The random sequence for 16-bit PRBS and 8-bit PRBS is developed through the pseudo method. Unlike conventional random sequences, the pseudo generator continues the random signal, and N elements later, the random signal repeats automatically and gives another set of random binary sequences in contrast to real random sequences, e.g., radioactive decay and white noise. It is executed using the linear feedback type of shift registers for getting the same probability order of ‘1’ s and ‘0’ s. The PRBS bit generator is a lead–lag random bit trainer, which is designed by using shift register and XOR gates. A more common form of LFSR is designed using a simple shift register getting feedback from two or more points or tapings available in the chain of registers.

The PRBS working in the below example is from the output of the first (bit 0) and third D-flip-flop (bit 2) of the 3-bit shift register. All the third D-flip-flops of the 3-bit shift register are triggered by the same clock signal. The input for LFSR is produced by XOR using bit 0 and bit 2 from the shift register. The rest of the D-flip-flop outputs are used only for the data-shifting function. The pattern or the sequence of bits produced is the result of the combined action of output produced by XOR and the choice of inputs of XOR.

This creates an *n*-bit shift register with a constant clock of frequency *f_c* generated with the help of a random carrier wave. The input for first D-flip flop is produced by the output of the XOR gate and is shifted in series to adjacent D-flip flops. The output of the XOR gate depends on the bits tapped from the D-flip flops and XOR operation. Random pulses are generated every *f_c* clock signal. The possible number of outputs is determined by $K = 2^n - 1$.

The PRBS with a random variable needed to choose the PP is attained from the XOR gate output. The random selection of triangular carrier wave having discrete frequency is generated from a pseudo-random carrier method. The logic behind 8-bit and 16-bit PRBS is shown in Figure 4. The output available from PRBS bits of the random bits generator is found as follows in Equations (1) and (2)

$$O_{PRBS-16bit} = B_{16} \oplus B_{14} \oplus B_{13} \oplus B_{11} \tag{1}$$

$$O_{\text{PRBS-8bit}} = B_8 \oplus B_6 \oplus B_5 \oplus B_4 \quad (2)$$

where B_x represents the x th output bit of the n -bit shift register and \oplus represents the XOR operator. When the output of the 8-bit PRBS generator becomes zero as well as the output of 16-bit PRBS generator becomes zero, the carrier having 2 kHz frequency is chosen. When there is zero output of the 16-bit PRBS generator and unity output of the 8-bit PRBS generator, a 3 kHz frequency carrier wave is chosen. When output of the 16-bit PRBS generator becomes one and that of the 8-bit PRBS generator becomes zero, a 4 kHz frequency carrier wave is chosen. When the output of the 16-bit PRBS generator becomes one and the output of the 8-bit PRBS generator becomes one, the carrier is determined to synthesize a random carrier wave. The random carrier wave generated is required for producing trigger gate pulses in VSI. The modulating signal is represented by three-phase reference signals. The proposed MCBRCPWM scheme waveforms are shown in Figure 4. The randomness of the PWM signals is a result of both the different randomization of carrier frequency and the bits from PRBS. This feature makes for an incessant distribution of the power spectra when compared with just the random frequency carrier scheme or the conventional scheme.

After creating a random signal, the multi-frequency random carrier signal is given to the SVPWM block. Here, the proposed SVPWM is alerted for adapting a random signal. The motor quantities (voltages and currents) can be given to the SVPWM reference generator, and these references are calculating the magnitude and phase angle of the SVD. In the SVPWM technique, the process of generating the pulse width command is reduced to a few simple equations. The basic idea behind SVPWM is the compensation of the required volt seconds by the use of discrete switching states and corresponding on-times (t_a and t_b) for switching. Figure 5 represents the 2-level inverter space vector diagram (SVD) and respective switching pulse [24]. Every sector of the SVD remains an equilateral triangle with height; $h (=3/2)$ is the height of a sector. The voltage vectors can be classified into two types: large vector (LV) and zero vector (ZV). Here, V_1 to V_6 vectors viz., $\{[100], [110], [010], [011], [001], \text{ and } [101]\}$ are active vectors and V_0, V_7 are zero vectors $\{(000), (111)\}$. Table 1 maps the switch status with the vectors.

The switching instants of SVPWM for six switch VSIs and switching cycles for sector-1 are shown in Figure 5. The on-time calculation for any of the six sectors (Δ_i) (where $i = 1, 2, 3, 4, 5$ and 6) is the same, and hence, the function of sector 1 is considered for understanding the complete SVD. V^* , the reference voltage, represents the rotating SVD form of three-phase voltage.

Table 1. SVPWM switching table.

Vector	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	V _{ab}	V _{bc}	V _{ca}	Vector
V ₀ = {000}	OFF	OFF	OFF	ON	ON	ON	0	0	0	Zero Vector
V ₁ = {100}	ON	OFF	OFF	OFF	ON	ON	+V _{dc}	0	−V _{dc}	Active Vector
V ₂ = {110}	ON	ON	OFF	OFF	OFF	ON	0	+V _{dc}	−V _{dc}	Active Vector
V ₃ = {010}	OFF	ON	OFF	ON	OFF	ON	−V _{dc}	+V _{dc}	0	Active Vector
V ₄ = {011}	OFF	ON	ON	ON	OFF	OFF	−V _{dc}	0	+V _{dc}	Active Vector
V ₅ = {001}	OFF	OFF	ON	ON	ON	OFF	0	−V _{dc}	+V _{dc}	Active Vector
V ₆ = {101}	ON	OFF	ON	OFF	ON	OFF	+V _{dc}	−V _{dc}	0	Active Vector
V ₇ = {111}	ON	ON	ON	OFF	OFF	OFF	0	0	0	Zero Vector

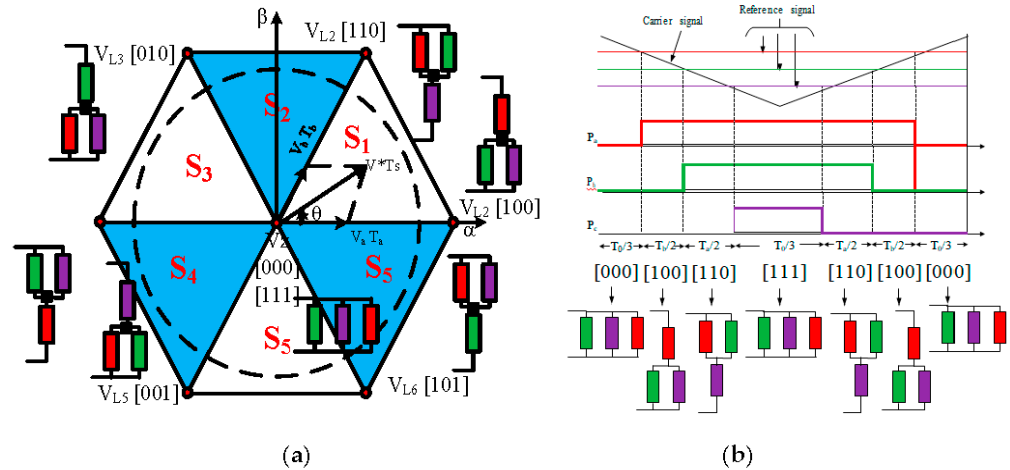


Figure 5. Space vector diagram switching state and respective switching pulse. (a). Space vector diagram switching state, (b) respective switching pulse for sector -1 .

The α - β plane projection of V^* during any period lies in any one of the sector areas. For instance, Figure 5 shows that V^* lies in the first sector edged by vector V_1 and V_2 . From time t_0 , V^* travels to t_1 and the relationship with the time integral is given as

$$\int_{t_0}^{t_1} V^* = T_a V_1 + T_b V_2 \tag{3}$$

$$V^* T_s = V_1 T_a + V_2 T_b \tag{4}$$

$$V_{\alpha 0}^s T_s = T_a + 0.5 T_b \tag{5}$$

$$V_{\beta 0}^s T_s = h T_b \tag{6}$$

From the above two Equations (5) and (6), the time durations T_a and T_b can be estimated.

$$T_b = T_s \left[\frac{V_{\beta 0}^s}{h} \right] \tag{7}$$

where $T_s (=1/f_s)$ is the sampling period. Thus, the T_a equation is redefined as

$$T_s = T_a + T_b + T_0 \tag{8}$$

Therefore, the time spent by the zero-vector state is

$$T_0 = T_s - T_a - T_b \tag{9}$$

where T_0 is turned to the zero state (off time of the switching).

The developed SVPWM is in agreement with the multicarrier (different fixed frequencies as carrier waves) and is chosen with the aid of a random binary bit generator. This contribution mainly deals with the combination of the multicarrier RPWM principle with space vector PWM (SVPWM) to generate multicarrier random space vector PWM (MCRSVPWM). The SVPWM is in agreement with multicarrier (different fixed frequencies as carrier waves) signals, which are chosen with the aid of a random binary bit generator. The proposed method generates pulses with a randomized triangular carrier (1 kHz, 2 kHz, 3 kHz, and 4 kHz), while the conventional RPWM method contains the random pulse position with a fixed frequency triangular carrier.

4. Simulation

The simulation study is done through the MATLAB/Simulink software tool (2016.b) for a three-phase VSI-connected 2 kW asynchronous induction motor. The simulation model of the proposed MCRSVPWM is shown in Figure 6. In this simulation, the major structure is with three main blocks: (1) reference signal generation, (2) random carrier generation, and (3) SVPWM pulse generation. After deciding the modulation index via a reference signal, the random carrier generation block will give the carrier signal to the SVPWM sampling and a holding block to compare the inverter pulses.

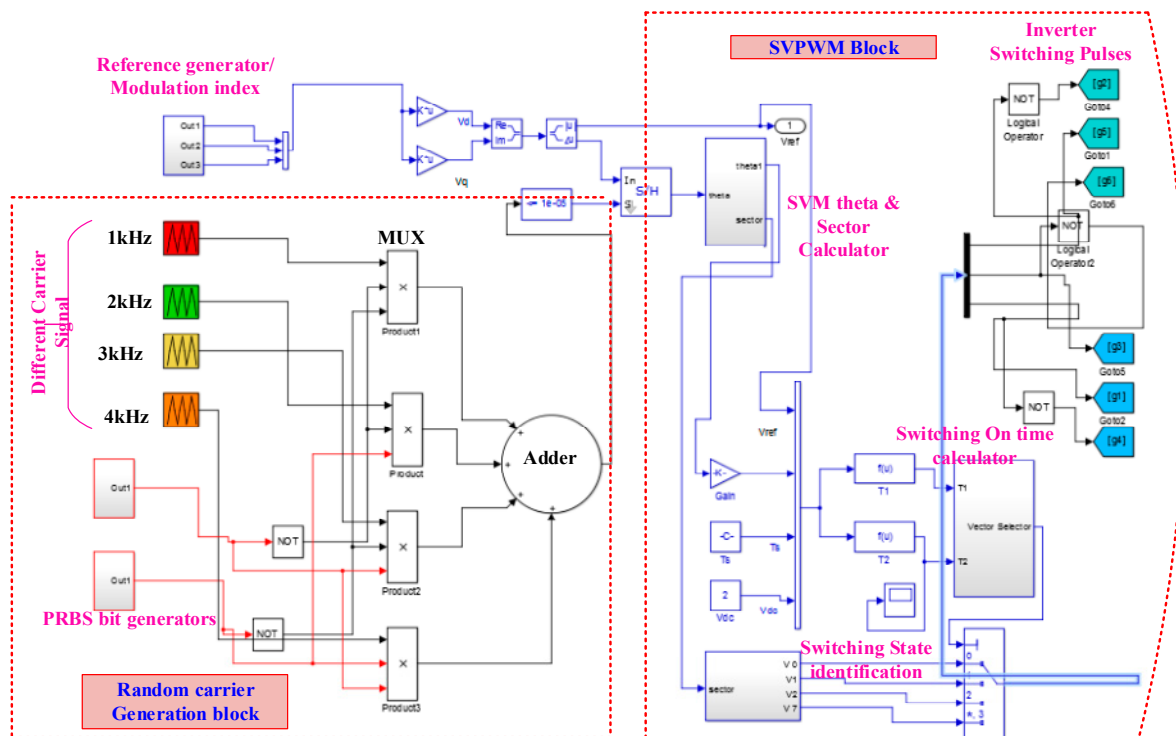


Figure 6. MATLAB simulation model for the MCRSVPWM.

The inverter is investigated with different RPPWM including the proposed MCRSVPWM. Initially, the VSI-connected conventional RPWM and RRPWM results are captured and compared with the proposed MCRSVPWM schemes. The switching frequencies of RCPWM are 1 kHz to 4 kHz; throughout the simulation, the DC-link voltage has been maintained as 400 V, and the inverter is operated in the range of the modulation index from 0.1 M_a to 0.9 M_a . When the multiple frequencies are fixed at the signal generator as 1 kHz, 2 kHz, 3 kHz, and 4 kHz, the analysis is taken. Around this frequency, the proposed RPWM eliminates the noise of the selective frequency, which is less than 20 kHz. Figure 7a–c shows the measured inverter line voltage under modulation index $M_a = 0.7$ and $M_a = 0.7$. During the condition, the inverter delivers the maximum permissible DC-link utilization. Figure 7b–d shows the voltage and its corresponding harmonics spectra with $M_a = 0.7$ and $M_a = 0.9$, respectively. Based on the results, it can be seen that the fundamental voltage is achieved linearly by changing the modulation index, and the harmonics spectra ($\%V_{THD}$) is validated as 47.6% and 51.5%, which is smaller than all the other reported RPWM values. Correspondingly, when the inverter is operating at lower modulation, it is in the M_a (low speed) operating region, due to the pulse dropping the V_{THD} , and I_{THD} is increasing. Table 2 shows all the corresponding results for different operating regions. From the results, it can be understood that the inverter not only reduces the THD but also maintains the DC-link utilization.

Table 2. Motor specifications.

Parameters	Values
Stator phase resistance, R_s	2.875 m Ω
Stator phase inductance, L_s	850 μ H
Pole pairs	4
DC supply voltage	100VDC
Current limit threshold	20A
DC bus capacitance C_1 and C_2	200 μ F
Inertia, viscous damping, static friction constants	0.8×10^{-3} J(kg·m ²), 1×10^{-3} F(N·m·s)

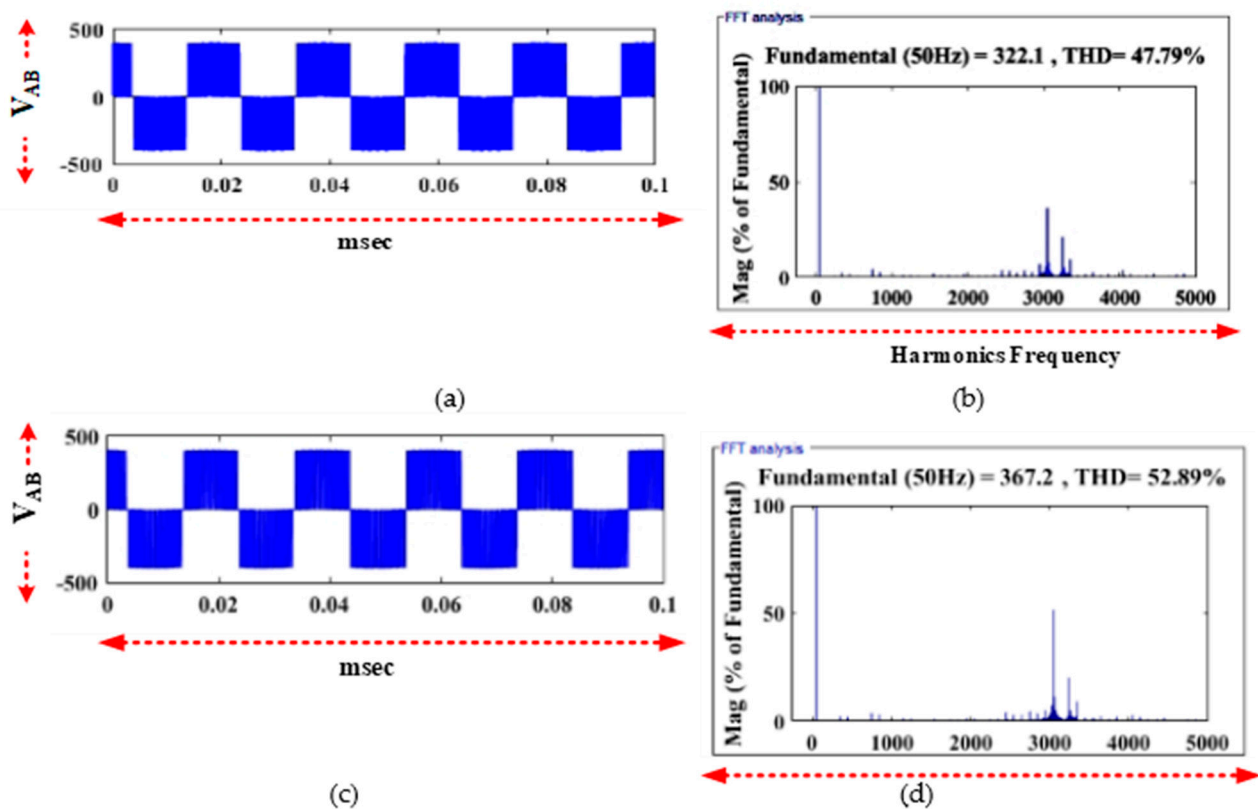


Figure 7. Simulation results MCRSVPWM: (a) Line voltage for $M_a = 0.7$, (b) Line voltage THD spectra for $M_a = 0.7$, (c) Line voltage for $M_a = 0.9$, (d) Line voltage THD spectra for $M_a = 0.9$.

Similar to the HSF of voltage, the current spectra must be calculated for any random PWM schemes for evaluating their noise calculation. This is a simple statistical deviation derived in [21,22].

$$HSF = \sqrt{\frac{1}{N} \sum_{j>1}^N (H_j - H_0)^2} \tag{10}$$

$$H_0 = \frac{1}{N} \sum_{j>1}^N (H_j) \tag{11}$$

Here, H_j = amplitude of j th harmonics and h_0 = the average value of all order harmonics. When HSF stays near zero, the white noise is zero. However, the zero HSF is partially not possible. On the other hand, the HSF is too small to allow a better harmonics spread. Hence, the proposed PWM coins the lesser HSF through a simple algorithm. The simulated values of different PWM methods including the proposed MCRSVPWM are compared through Table 3. The tables are focusing on the fundamental voltage and current, voltage THD, and HSF. The proposed MCRSVPWM shows its victory by means of the working range when compared with the other five cases. When $M_a = 0.8$, about a 42% reduction of HSF is achieved from RPWM and SPWM, 36% reduction is achieved from chaotic PWM,

14% reduction is achieved from RPPPWM, and 21% reduction is achieved from RCPWM. The values of V_1 and THD are not highly disturbed for the five cases, except for the non-deterministic RPWM, where about 48% of reduction in V_1 is observed. The simulations (see Figure 8a–d) were made for the four speed values of the motor, which is achieved by setting the different values of modulation indices (for $M_a = 0.2$, $M_a = 0.5$, $M_a = 0.7$, and $M_a = 0.9$). During the low-speed range, similar to RSWM, the proposed RSVPWM shows good performance by means of the disappearance of discrete frequency components from the spectrum around the switching frequency; nevertheless, the discrete components exist. In medium speed to high speed, the proposed SVPWM has a better performance than all the other reported PWM.

Table 3. Simulation study and HSF results comparisons.

M_a /HSF	SPWM (HSF)	RPWM (HSF)	CPWM (HSF)	RCRPWM (HSF)	MRCRPWM (HSF)	Proposed MCRSVPWM (HSF)
0.1	9.21	9.11	6.26	6.54	4.32	4.12
0.2	8.31	8.11	6.09	6.26	4.12	4.03
0.3	7.56	7.42	6.02	6.12	4.01	3.89
0.4	6.14	6.03	6.03	6.11	3.95	3.76
0.5	6.89	6.56	5.00	5.19	3.91	3.65
0.6	5.88	5.31	4.56	4.71	3.71	3.56
0.7	5.69	5.12	4.21	4.56	3.43	3.29
0.8	5.57	5.07	3.95	4.25	3.23	3.00
0.9	5.16	4.98	3.25	3.56	3.02	2.86

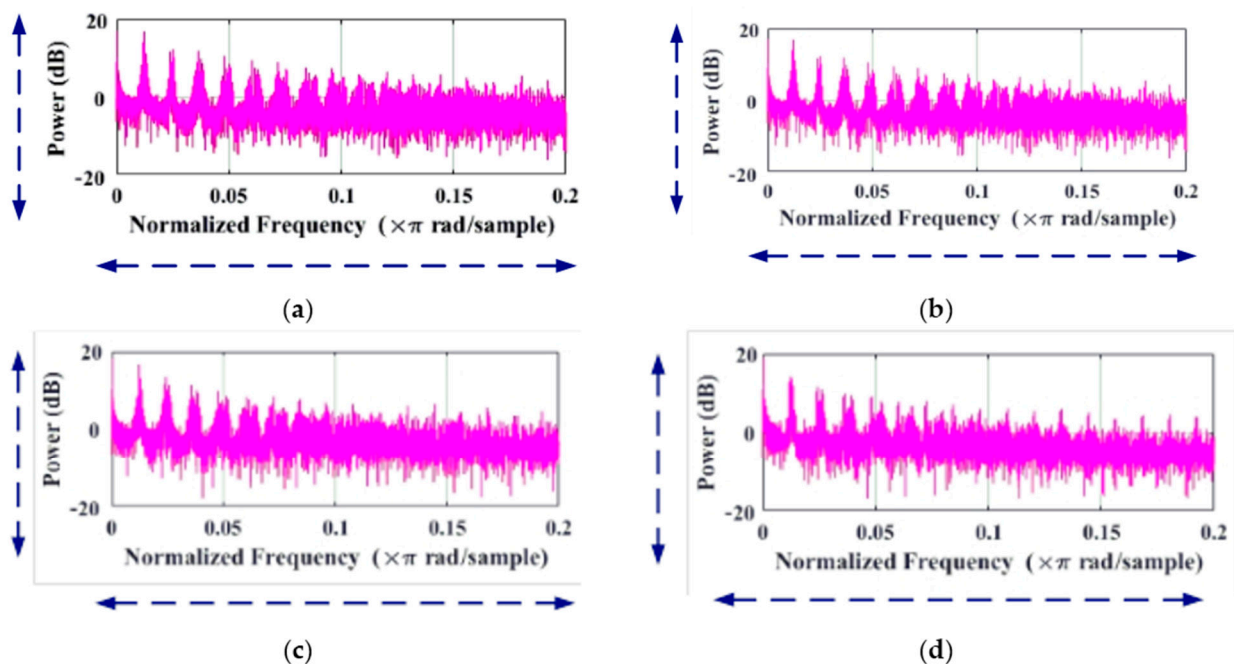


Figure 8. MCRSVPWM simulation results of motor current spectrum for M_a values: (a) $M_a = 0.2$, (b) $M_a = 0.5$, (c) $M_a = 0.7$, and (d) $M_a = 0.9$.

The proposed PWM completely removes the discrete components, and the discrete components of the current spectrum are located around the switching frequency, which can be easily limited by a simple filter. Table 3 shows the comparison of HSF for all the reported RPWM with proposed MCRSVPWM. From the table, it is clearly seen that the MCRSVPWM has less HSF throughout the inverter operation. The reason behind this is that most of the dominant frequency component is considerably reduced by spreading

the carrier frequency; hence, the non-fundamental power is spread out in an ample wider frequency, which helps reduce the acoustic noise.

Table 4 shows the simulation study results for the line voltage and line voltage THD for the SPWM, RPWM, CPWM, RCRPWM, and MRCRPWM, including the proposed MCRSVPWM method. Here, it can be seen that the proposed MCRSVPWM has a better line voltage and THD compared to the other methods.

Table 4. Simulation study results comparing the line voltage and line voltage THD for the proposed MCRSVPWM with the other reported RPWM methods.

M_a	SPWM		RPWM		CPWM		RCRPWM		MRCRPWM		MCRSVPWM	
	V_1 (Volts)	% V_{THD}	V_1 (Volts)	% V_{THD}	V_1 (Volts)	% V_{THD}	V_1 (Volts)	% V_{THD}	V_1 (Volts)	% V_{THD}	V_1 (Volts)	% V_{THD}
0.1	24	59.56	17	53.36	25	55.11	25	59.12	29	51.12	29	50.54
0.2	55	54.82	43	49.82	56	51.84	56	54.42	58	47.49	59	46.87
0.3	81	53.21	62	47.21	83	52.54	83	53.01	89	45.67	90	44.51
0.4	111	45.22	85	48.22	114	49.92	114	45.08	117	46.25	120	44.99
0.5	139	46.06	112	51.06	142	50.35	142	45.52	146	49.25	149	47.98
0.6	165	47.07	126	52.07	169	54.78	168	46.14	175	52.56	179	51.16
0.7	194	54.41	156	54.41	189	56.21	197	54.41	204	52.06	207	51.04
0.8	215	56.92	189	55.92	225	56.59	219	55.14	233	53.08	236	51.87
0.9	248	59.45	215	56.454	253	56.18	257	58.43	263	53.54	267	52.89

The inverter switches need to be rated to withstand the peak magnitude of the input DC-link voltage and the maximum expected output voltage, and they should be able to safely dissipate the heat generated in the switch due to conduction and switching losses. As a result of high-frequency switching, the switches in the PWM inverters have significantly more switching loss than in square wave inverters. Often, the switch chosen in the PWM inverters is oversized, in terms of its current rating, so that the sum total of switching loss and conduction loss remains well within the heat dissipation capability of the switch and the associated net output voltage. Hence, based on the PWM pulse arrangement, the output voltage of the inverter is varied.

In this study, the proposed MCRSVPWM used SVPWM, where the maximum DC-link voltage is achieved. Other PWM methods used for the comparisons except for regular SVPWM (without RPWM) are similar to that of sine PWM arrangement. Hence, for the given modulation index, the inverter line voltage is higher in the proposed MCRSVPWM and MRCRPWM. The variation in the voltage is verified and the comparison table is revised.

The random carrier pulse width modulation (RCPWM) practice is basically related to conventional SPWM with the variation in their carrier frequencies. In this method, two prerequisite frequency triangular carriers with 180-degree phase shifting are used to create the randomness on the resultant carrier. Hence, the noise of the inverter output is reduced. However, any random carriers affect the inverter DC-link utilization. Compared to sine PWM, space vector PWM has a superior quality to provide an operating region to 90.07% (maximum modulation index, $m_a = 0.907$). Hence, the RCPWM is merged with space vector PWM, which helps spread the noise harmonics around the inverter switching spectra with better DC utilization. In addition, with RPWM and space vector PWM, the proposed random carrier pulse width modulation (RCPWM) is used with multi-carrier (different fixed frequencies as carrier waves) and is chosen with the aid of a random binary bit generator. The proposed method generates pulses with a randomized triangular carrier (1 kHz, 2 kHz, 3 kHz, and 4 kHz), while the conventional RPWM method contains the random pulse position with a fixed frequency triangular carrier. Table 5 shows the DC-link utilization (as a line voltage), the percentage voltage of THD, and HSF. From the table, it is well understood that during the entire inverter operating condition, the proposed MCRSVPWM maintains the voltage THD better than the other reported PWM

schemes from the literature as well as maintains the DC-link utilization of the inverter with better HSF.

Table 5. The combined comparisons of line voltage and line voltage THD and HSF study results.

M_a	SPWM			RPWM			RCRPWM			MRCRPWM			MCRSVPWM		
	V1 (Volts)	% V_{THD}	HSF	V1 (Volts)	% V_{THD}	HSF	V1 (Volts)	% V_{THD}	HSF	V1 (Volts)	% V_{THD}	HSF	V1 (Volts)	% V_{THD}	HSF
0.1	27.1	59.56	9.21	27.2	53.36	9.11	27.6	59.12	6.54	28.1	51.12	4.32	29	50.54	4.12
0.2	56.5	54.82	8.31	56.8	49.82	8.11	57.9	54.42	6.26	58	47.49	4.12	59	46.87	4.03
0.3	86.8	53.21	7.56	87.1	47.21	7.42	88.2	53.01	6.12	89.1	45.67	4.01	90	44.51	3.89
0.4	115.9	45.22	6.14	116.3	48.22	6.03	117.3	45.08	6.11	118.6	46.25	3.95	120	44.99	3.76
0.5	144.9	46.06	6.89	145.6	51.06	6.56	146.8	45.52	5.19	147.8	49.25	3.91	149	47.98	3.65
0.6	174.1	47.07	5.88	174.9	52.07	5.31	176.8	46.14	4.71	177.8	52.56	3.71	179	51.16	3.56
0.7	200.3	54.41	5.69	201.1	54.41	5.12	204.3	54.41	4.56	206.1	52.06	3.43	207	51.04	3.29
0.8	215.6	56.92	5.57	220.1	55.92	5.07	229.5	55.14	4.25	233.6	53.08	3.23	236	51.87	3.00
0.9	255.4	59.45	5.16	256.3	56.454	4.98	259.9	58.43	3.56	264.5	53.54	3.02	267	52.89	2.86

5. Experimental Validation

An experimental setup is built in order to validate the simulation results of the proposed induction motor (IM) drive. The experimental setup and design flow of the FPGA implementation design flow for MCRSVPWM is shown in Figures 9 and 10, respectively.

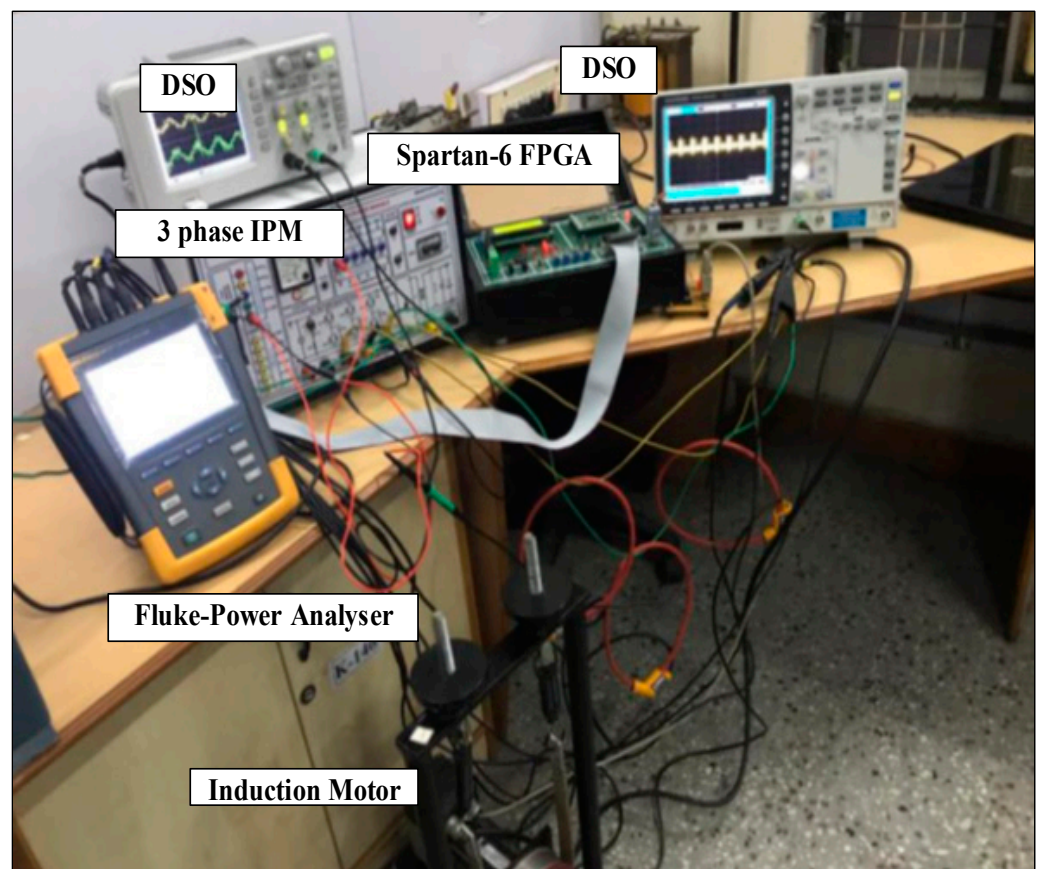


Figure 9. Laboratory-scale experimental setup of three-phase VSI-connected induction motor drive.

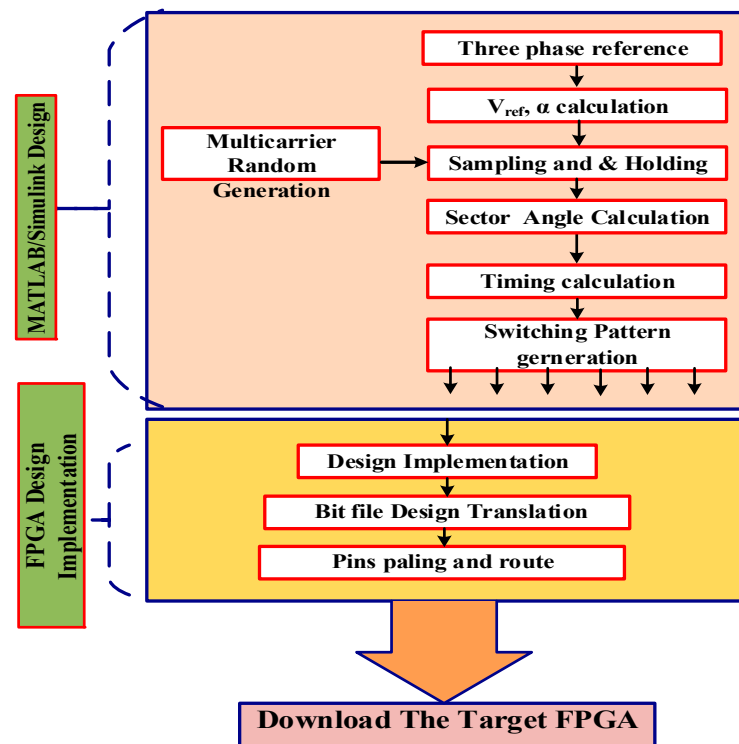


Figure 10. Design flow of FPGA implementation on MCRSVPWM.

Experimental validation of the proposed RPWM is tested with the VSI-fed induction motor. The experimental setup of the three-phase VSI connected induction motor drive is shown in Figure 9. A 2 kW six switch (Power MOSFET-SCH2080KE) inverter power module is used as a VSI and the 3HP, three-phase induction motor is used for the experimentation. The inverter used a 3400 microF DC-link capacitor to maintain the DC bus voltage as 400 V. The random carrier (1 to 4 kHz) and SVPWM is developed using the Xilinx-MATLAB system generator tool, and the bit file is generated and downloaded in a Spartan-6 FPGA controller. The multicarrier signals are generated using ramp logic code using VHDL and stored using a FPGA look-up table (LTU) [40]. The different carrier frequencies are mixed through a PRPS generating random binary and given to the SVPWM block. The dead time is fixed for an inverter leg as 6 microseconds. The VSI-fed IM drive is tested for different frequency combinations for changing the sequences of the mixer of carrier frequencies. The SVPWM block is designed to support the variation of the inverter modulation index M_a between 0 and 0.9. Figure 11 shows the inverter experimental results of switching the pulses of the MCRSVPWM-fed VSI for $M_a = 0.9$.

Initially, the inverter is tested for the frequencies without floating combinations as $f_{c1} = 1$ kHz, $f_{c2} = 2$ kHz, $f_{c3} = 3$ kHz, and $f_{c4} = 4$ kHz. Figures 12 and 13 show the inverter operating line voltage and voltage harmonics performance at $M_a = 0.6$ and $M_a = 0.9$. It is illustrating the line-to-line voltage of V_{AB} and its percentage V_{THD} of $M_a = 0.6$ and $M_a = 0.9$. When the inverter drive is operating at medium speed ($M_a = 0.6$), the V_{AB} and its THD are observed as 173 V and 51.6%, respectively. Similarly, when the inverter is operating at a higher modulation index, $M_a = 0.9$ operating region, the line-to-line voltage, V_{AB} is increasing linearly to 262.5 V, and its percentage V_{THD} is recovered as 51.7%. From these results, it can be understood that during the entire inverter operating condition proposed, MCRSVPWM maintains the voltage THD better than the other reported RPWM schemes and also maintains the DC-link utilization of the inverter.

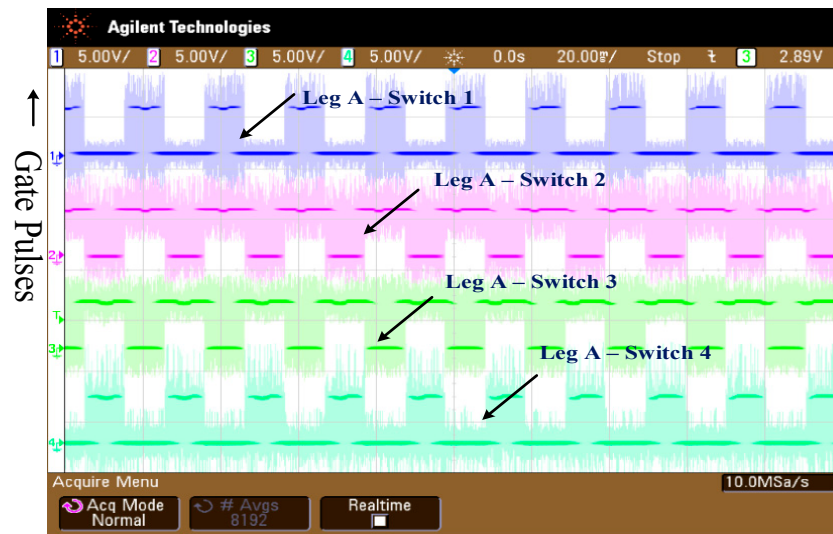


Figure 11. Excremental results of switching pulses of MCRSVPWM-fed VSI for $M_a = 0.9$.

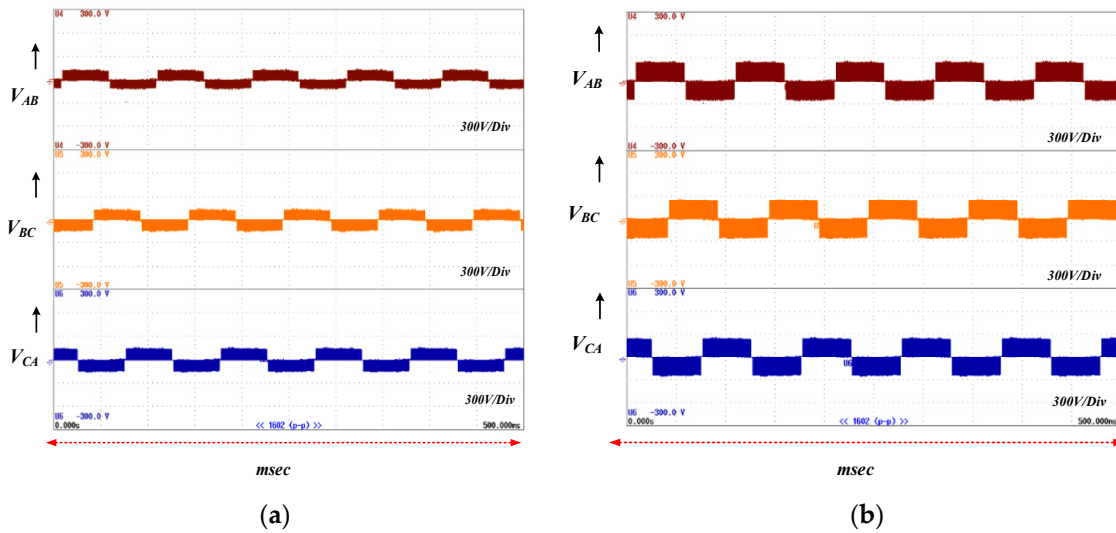


Figure 12. Excremental results MCRSVPWM: (a) Line voltage for $M_a = 0.6$, (b) Line voltage (V_{AB}) for $M_a = 0.9$.

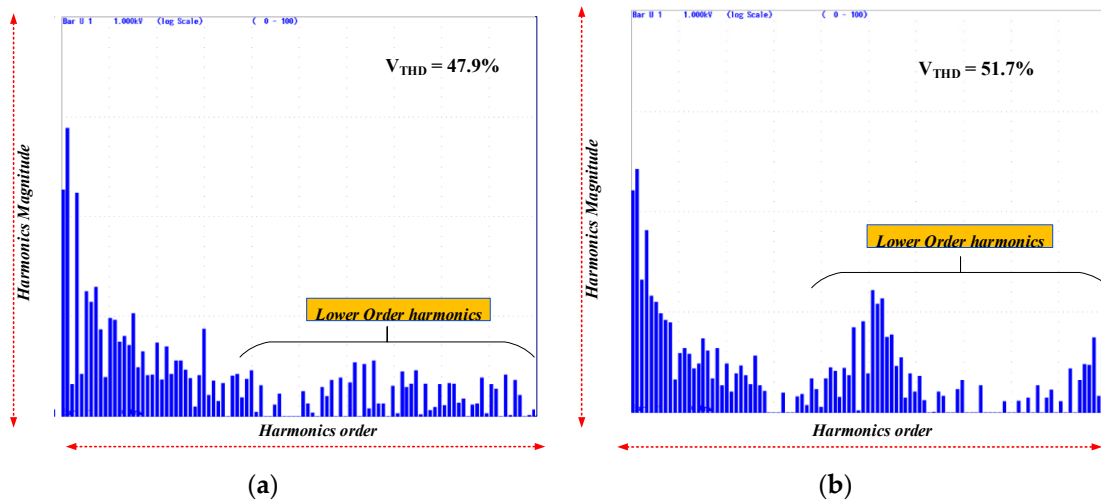


Figure 13. Excremental results MCRSVPWM: (a) Harmonics spectrum of V_{AB} at $M_a = 0.6$, (b) Harmonics spectrum of V_{AB} at $M_a = 0.9$.

The different hardware results with respect to different modulation conditions are reordered and given in Table 6. The hardware results confirm the simulation results. The MCRSVPWM confirms the superiority of their reduction of noise (HFS %) and better DC-link utilizations.

Table 6. Experimental study results for the MCRSVPWM.

M_a	SPWM (HSF)	RPWM (HSF)	CPWM (HSF)	RCRPWM (HSF)	MRCRPWM (HSF)	Proposed MCRSVPWM (HSF)
0.1	9.24	9.16	6.29	6.58	4.32	4.15
0.2	8.35	8.15	6.13	6.29	4.12	4.07
0.3	7.59	7.46	6.06	6.17	4.01	3.94
0.4	6.18	6.08	6.05	6.15	3.99	3.85
0.5	6.93	6.59	5.05	5.23	3.96	3.75
0.6	5.92	5.36	4.59	4.75	3.76	3.64
0.7	5.72	5.17	4.25	4.59	3.48	3.39
0.8	5.60	5.11	3.99	4.29	3.28	3.07
0.9	5.20	5.02	3.28	3.59	3.08	2.95

Comparisons of simulation and experimental results are given in Figure 14. Figure 14a shows the line voltage versus the modulation index, and Figure 14b shows the reduction of noise (HFS %) versus the modulation index. Figure 14a shows that the simulation line voltage is slightly higher than the experimental line voltage. This is due to the switching and conduction losses in real-time experimentation factors. The noise HFS% is slightly higher in the experimental results against all modulation indices. This is due to the higher harmonics that appeared in the experimentation.

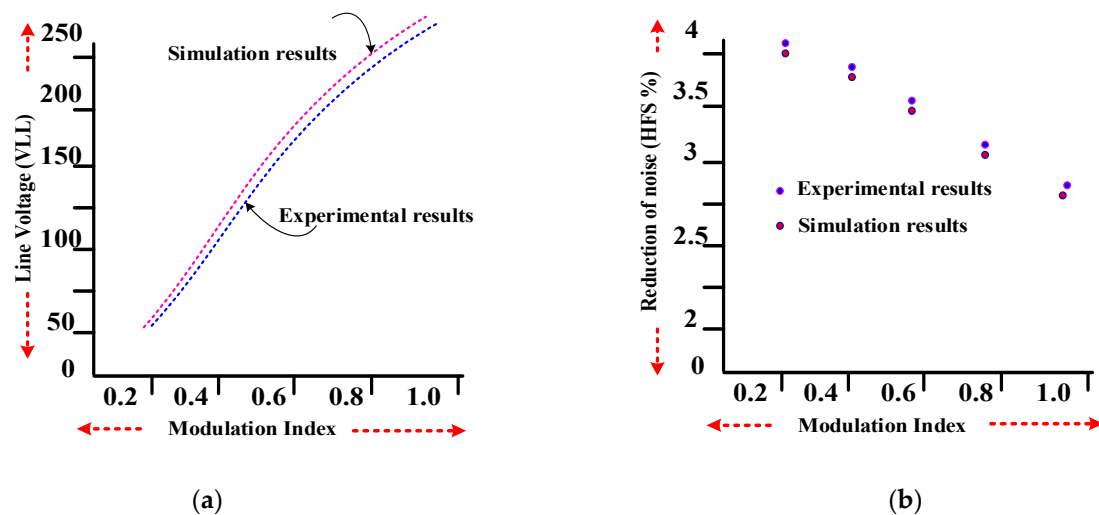


Figure 14. Comparisons of simulation and experimentation: (a). Line voltage versus modulation index, (b) Reduction of noise (HFS %) versus modulation index.

The proposed MCRSVPWM can be used in various applications such as drives and power system power quality improvement. The proposed random PWM is able to reduce the acoustic noise and electromagnetic interference in VSI-fed motor drives. It also can be extended for CSI drives such as current controlled and Direct Torque Control (DTC) AC drives. The time for zero voltage is randomized to get better results with Direct Torque Control (DTC) for drives. The proposed MCRSVPWM can help flatten the power density spectrum of the drive, reduce switching loss, decrease current ripple, and auto-adjust load characteristics. The proposed RPWM can be used to reduce the particular acoustic noise and electromagnetic noise. Hence, it can be used for dynamic load characteristics applications

such as electrical vehicles' drives and automobiles' AC motor drives (induction motor and PMSM motor drives). In shunt active power filter is used to improve power quality issues such as current harmonics and power factor for a power system with nonlinear load. With random PWM, the APF response can be improved without adding any cost.

6. Conclusions

In this paper, a multicarrier random space vector PWM was presented for a three-phase two-level six switch voltage source inverter-fed induction motor. The proposed multiple carrier-based random method improves the randomness, which helps spread the harmonics around the spectra. The SVPWM agrees with multicarrier (different fixed frequencies as carrier waves), which are chosen with the aid of a random binary bit generator. The proposed MCRSVPWM generated pulses with a randomized triangular carrier (1 to 4 kHz), while the conventional RPWM method contains the random pulse position with a fixed frequency triangular carrier. The FPGA-based two PRBS bit (8 bit and 16 bit) generators are used to generate the random binary for getting random carriers for the pulse generations. The simulation study is performed through MATLAB/Simulink for a 2.5A asynchronous induction motor drive. The experimental validation of the proposed RSVM is tested with a 2 kW six switch (Power MOSFET-SCH2080KE) inverter power module-fed induction motor drive. The MCRSVPWM is confirming the superiority of their reduction of noise and better DC-link utilizations. The proposed PWM is capable of eradicating the high-frequency unpleasant acoustic noise more effectually than a conventional RPWM with a shorter random frequency range.

The proposed MCRSVPWM can be used in drives and a power system shunt active power filter to improve the power quality. The proposed random PWM is able to reduce the acoustic noise and electromagnetic interference VSI-fed motor drives. The proposed MCRSVPWM can help flatten the power density spectrum of the drive, reduce the switching loss, decrease the current ripple, and auto-adjust load characteristics. The proposed RPWM can be used to reduce the particular acoustic noise and electromagnetic noise. Hence, it can be used for dynamic load characteristics applications such as electrical vehicles drives.

Author Contributions: Conceptualization, P.M., C.B. and R.V.; methodology, P.M., C.B., J.L.M. and R.V.; software, J.L.M., C.B. and T.S.; validation, P.M., C.B. and L.M.-P.; formal analysis, J.L.M., C.B. and R.V.; investigation, P.M., C.B. and R.V.; resources, J.L.M., R.V., B.P.G.J.; data curation, P.M., C.B. and R.V.; writing—original draft preparation, P.M., C.B. and R.V.; writing—review and editing, B.P.G.J. and J.L.M.; visualization, B.P.G.J.; supervision, R.V., C.B. and J.L.M.; project administration, R.V.; funding acquisition, J.L.M. and R.V. All authors have read and agreed to the published version of the manuscript.

Funding: This research is associated with Deanship of Scientific Research at King Khalid University, Kingdom of Saudi Arabia for funding this work through General Research Project under the grant number (RGP. 1/262/42).

Data Availability Statement: Experimental data is available upon request.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ghodke, D.V.; Chatterjee, K.; Fernandes, B.G. Three-Phase Three Level, Soft Switched, Phase Shifted PWM DC–DC Converter for High Power Applications. *IEEE Trans. Power Electron.* **2008**, *23*, 1214–1227. [[CrossRef](#)]
2. Kaboli, S.; Mahdavi, J.; Agah, A. Application of Random PWM Technique for Reducing the Conducted Electromagnetic Emissions in Active Filters. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2333–2343. [[CrossRef](#)]
3. Ojo, O. The Generalized Discontinuous PWM Scheme for Three-Phase Voltage Source Inverters. *IEEE Trans. Ind. Electron.* **2004**, *51*, 1280–1289. [[CrossRef](#)]
4. Bharatiraja, C.; Jeevananthan, S.; Latha, R.; Mohan, V. Vector selection approach-based hexagonal hysteresis space vector current controller for a three phase diode clamped MLI with capacitor voltage balancing. *IET Power Electron.* **2016**, *9*, 1350–1361. [[CrossRef](#)]

5. Li, G.; Liu, C.; Fu, Z.; Wang, Y. A Novel RPWN Selective Harmonic Elimination Method for Single-Phase Inverter. *Electronics* **2020**, *9*, 489. [[CrossRef](#)]
6. Jacob, B.; Baiju, M.R. Spread spectrum modulation scheme for two-level inverter using vector quantised space vector-based pulse density modulation. *IET Electr. Power Appl.* **2011**, *5*, 589. [[CrossRef](#)]
7. Kim, K.-S.; Jung, Y.-G.; Lim, Y.C. A New Hybrid Random PWM Scheme. *IEEE Trans. Power Electron.* **2009**, *24*, 192–200. [[CrossRef](#)]
8. Bharatiraja, C.; Prasad, T.B.; Latha, R. Comparative realization of different SVPWM schemes in linear modulation using FPGA. In Proceedings of the 2008 IEEE Region 8 International Conference on Computational Technologies in Electrical and Electronics Engineering, Novosibirsk, Russia, 21–25 July 2008; pp. 164–168.
9. Kragh, H.; Blaabjerg, F.; Pedersen, J.K. Reduce of the acoustic noise effect from PWM-VSI inverter controlled AC-drives by music and random modulation. In Proceedings of the Conference Record of the Power Conversion Conference, Yokohama, Japan, 19–21 April 1993; pp. 369–375.
10. Lim, Y.-C.; Wi, S.-O.; Kim, J.-N.; Jung, Y.-G. A Pseudorandom Carrier Modulation Scheme. *IEEE Trans. Power Electron.* **2009**, *25*, 797–805. [[CrossRef](#)]
11. Mathe, L.; Lungeanu, F.; Sera, D.; Rasmussen, P.O.; Pedersen, J.K. Spread Spectrum Modulation by Using Asymmetric-Carrier Random PWM. *IEEE Trans. Ind. Electron.* **2011**, *59*, 3710–3718. [[CrossRef](#)]
12. Borisov, K.; Calvert, T.; Kleppe, J.; Martin, E.; Trzynadlowski, A. Experimental investigation of a naval propulsion drive model with the PWM-based attenuation of the acoustic and electromagnetic noise. *IEEE Trans. Ind. Electron.* **2006**, *53*, 450–457. [[CrossRef](#)]
13. Schulz, S.E.; Kowalewski, D.L. Implementation of Variable-Delay Random PWM for Automotive Applications. *IEEE Trans. Veh. Technol.* **2007**, *56*, 1427–1433. [[CrossRef](#)]
14. Wang, Z.; Chau, K.T.; Liu, C. Improvement of Electromagnetic Compatibility of Motor Drives Using Chaotic PWM. *IEEE Trans. Magn.* **2007**, *43*, 2612–2614. [[CrossRef](#)]
15. Trzynadlowski, A.; Borisov, K.; Li, Y.; Qin, L. A Novel Random PWM Technique with Low Computational Overhead and Constant Sampling Frequency for High-Volume, Low-Cost Applications. *IEEE Trans. Power Electron.* **2005**, *20*, 116–122. [[CrossRef](#)]
16. Paramasivan, M.; Paulraj, M.M.; Balasubramanian, S. Assorted carrier-variable frequency-random PWM scheme for voltage source inverter. *IET Power Electron.* **2017**, *10*, 1993–2001. [[CrossRef](#)]
17. Habetler, T.; Divan, D. Acoustic noise reduction in sinusoidal PWM drives using a randomly modulated carrier. *IEEE Trans. Power Electron.* **1991**, *6*, 356–363. [[CrossRef](#)]
18. Shrivastava, Y.; Sathiakumar, S.; Hui, S. Improved spectral performance of random PWM schemes with weighted switching decision. *IEEE Trans. Power Electron.* **1998**, *13*, 1038–1045. [[CrossRef](#)]
19. Kim, J.-G.; Jung, Y.-G.; Na, S.-H.; Lim, Y.-C. A new random PWM(SRP-PWM) technique for decreasing acoustic noise radiated from V/F controlled motor drives. In Proceedings of the 30th Annual Conference of IEEE Industrial Electronics Society, Busan, Korea, 2–6 November 2004; pp. 832–837.
20. Lin, B.-R. Implementation of nondeterministic pulsewidth modulation for inverter drives. *IEEE Trans. Aerosp. Electron. Syst.* **2000**, *36*, 482–490. [[CrossRef](#)]
21. Zhang, Z.; Chau, K.T.; Wang, Z.; Li, W. Improvement of Electromagnetic Compatibility of Motor Drives Using Hybrid Chaotic Pulse Width Modulation. *IEEE Trans. Magn.* **2011**, *47*, 4018–4021. [[CrossRef](#)]
22. Lai, Y.-S.; Chen, B.-Y. New Random PWM Technique for a Full-Bridge DC/DC Converter with Harmonics Intensity Reduction and Considering Efficiency. *IEEE Trans. Power Electron.* **2013**, *28*, 5013–5023. [[CrossRef](#)]
23. Jiang, D.; Wang, F. Variable Switching Frequency PWM for Three-Phase Converters Based on Current Ripple Prediction. *IEEE Trans. Power Electron.* **2013**, *28*, 4951–4961. [[CrossRef](#)]
24. Lai, Y.-S.; Chang, Y.-T.; Chen, B.-Y. Novel Random-Switching PWM Technique with Constant Sampling Frequency and Constant Inductor Average Current for Digitally Controlled Converter. *IEEE Trans. Ind. Electron.* **2012**, *60*, 3126–3135. [[CrossRef](#)]
25. Mathe, L.; Rasmussen, P.O.; Pedersen, J.K. Shaping the spectra of the line-to-line voltage using signal injection in the common mode voltage. In Proceedings of the 2009 35th Annual Conference of IEEE Industrial Electronics, Porto, Portugal, 3–5 November 2009; pp. 1288–1293.
26. Zheng, J.; Lyu, M.; Li, S.; Luo, Q.; Huang, K. Common-Mode Reduction SVPWM for Three-Phase Motor Fed by Two-Level Voltage Source Inverter. *Energies* **2020**, *13*, 3884. [[CrossRef](#)]
27. Oh, S.-Y.; Jung, Y.-G.; Yang, S.-H.; Lim, Y.-C. Harmonic-Spectrum Spreading Effects of Two-Phase Random Centered Distribution PWM (DZRCD) Scheme with Dual Zero Vectors. *IEEE Trans. Ind. Electron.* **2009**, *56*, 3013–3020. [[CrossRef](#)]
28. Zhu, Y.; Guo, Z.; Han, B. An Improved Asymmetrical PWM Controlled Full Bridge DC-DC Converter for Circulating Current Reduction. In Proceedings of the 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 29 November–2 December 2020.
29. Selvaraj, R.; Desingu, K.T.; Chelliah, R.; Khare, D.; Bharatiraja, C. Fault Tolerant Operation of Parallel-Connected 3L-Neutral-Point Clamped Back-to-Back Converters Serving to Large Hydro-Generating Units. *IEEE Trans. Ind. Appl.* **2018**, *54*, 5429–5443. [[CrossRef](#)]
30. Xu, J.; Zhang, H. Random Asymmetric Carrier PWM Method for PMSM Vibration Reduction. *IEEE Access* **2020**, *8*, 109411–109420. [[CrossRef](#)]

31. Ruiz-Gonzalez, A.; Vargas-Merino, F.; Heredia-Larrubia, J.R.; Meco-Gutierrez, M.J.; Perez-Hidalgo, F. Application of Slope PWM Strategies to Reduce Acoustic Noise Radiated by Inverter-Fed Induction Motors. *IEEE Trans. Ind. Electron.* **2012**, *60*, 2555–2563. [[CrossRef](#)]
32. Pu, T.; Bu, F.; Huang, W.; Zhu, L. Implementation of random SVPWM strategy for three-phase voltage source inverter based on FPGA. In Proceedings of the 2017 20th International Conference on Electrical Machines and Systems (ICEMS), Sydney, Australia, 11–14 August 2017; pp. 1–4.
33. Bharatiraja, C.; Jeevananthan, S.; Munda, J.L. A Timing Correction Algorithm-Based Extended SVM for Three-Level Neutral-Point-Clamped MLI in Over Modulation Zone. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 233–245. [[CrossRef](#)]
34. Kumar, K.V.; Michael, P.A.; John, J.P.; Kumar, D.S.S. Simulation and comparison of SPWM and SVPWM control for three-phase inverter. *ARPJ. Eng. Appl. Sci.* **2010**, *5*, 61–74.
35. Huang, Y.; Xu, Y.; Zhang, W.; Zou, J. Hybrid RPWM Technique Based on Modified SVPWM to Reduce the PWM Acoustic Noise. *IEEE Trans. Power Electron.* **2019**, *34*, 5667–5674. [[CrossRef](#)]
36. Bharatiraja, C.; Selvaraj, R.; Chelliah, T.R.; Munda, J.L.; Tariq, M.; Maswood, A.I. Design and Implementation of the Fourth Arm for Elimination of Bearing Current in NPC-MLI-Fed Induction Motor Drive. *IEEE Trans. Ind. Appl.* **2018**, *54*, 745–754. [[CrossRef](#)]
37. Huang, Y.; Xu, Y.; Zhang, W.; Zou, J. Hybrid periodic carrier frequency modulation technique based on modified SVPWM to reduce the PWM noise. *IET Power Electron.* **2019**, *12*, 515–520. [[CrossRef](#)]
38. Huang, Y.; Xu, Y.; Zhang, W.; Zou, J. PWM frequency voltage noise cancellation in three-phase VSI using the novel SVPWM strategy. *IEEE Trans. Power Electron.* **2018**, *33*, 8596–8606. [[CrossRef](#)]
39. Selvaperumal, M.; Kirubakaran, D.; Bharatiraja, C. A hybrid space vector modulation for the near zero common mode voltage and common mode current mitigation in diode clamped multilevel inverter fed induction motor drive. *Int. Trans. Electr. Energy Syst.* **2020**, *30*. [[CrossRef](#)]
40. Lee, K.; Shen, G.; Yao, W.; Lu, Z. Performance Characterization of Random Pulse Width Modulation Algorithms in Industrial and Commercial Adjustable-Speed Drives. *IEEE Trans. Ind. Appl.* **2017**, *53*, 1078–1087. [[CrossRef](#)]