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RESEARCH ARTICLE

A Transformerless Non-Isolated Multi-Port DC–DC Converter for Hybrid Energy Applications

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ABSTRACT This paper presents a novel high-gain non-isolated Four Port DC-DC converter (FPC) topology for hybrid energy applications. The proposed four-port dc-dc converter interfaces four power ports of three input ports and one output port. High output voltage gain, minimized component count, and high efficiency are the advantages of the proposed converter, which renders it very useful for hybrid energy applications such as fast-charging electric vehicles. The high output voltage gain of the proposed FPC is achieved by the Actively Switched Inductor Capacitor (ALC) network. Moreover, the reduction in component count is achieved by minimizing the number of switches per input port. This enhances the converter efficiency is 96.77 % with a voltage gain 4.75. In this study, the FPC topology and modes of operation are described along with complete, steady state analysis, loss analysis, and switch voltage stress (VS) analysis of the converter. The converter operates in five modes, where all three sources can either be interfaced with the load by simply altering the switching patterns. Circuit topology, modes of operation, circuit analysis simulation, and real-time validations have been described in this paper.

INDEX TERMS DC–DC converter, four-port converter, reduction of switch voltage stress, voltage gain boost.

I. ABBREVIATION

ALC	Actively Switched Inductor Capacitor.
DIDO	Dual Input Dual Output.
DISO	Dual Input Single output.
DC	Direct Current.
EV	Electric Vehicle.
FPC	Four Port Converter.
HEV	Hybrid Electric Vehicle.
MDC	Maximum Demand Control.
MIMO	Multi Input Multi Output.
MPC	Multiport DC-DC Converters.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
MPPT	Maximum PowerPoint Tracking.
PV	Photovoltaic.
SC	Switched Capacitor.
SCL	Series Coupled Inductors.
SI	Single Inductor.
SIDO	Single Input Dual Output.
SL	Switched Inductor.
SCVMCs	Switched Capacitor Voltage Multiplier Cells.
SLVMCs	Switched Inductor Voltage Multiplier Cells.
VMCs	Voltage Multiplier Cell.
VS	Voltage Stress.

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II. INTRODUCTION

Due to the multiple environmental, societal, and health benefits, there has been a steady increase in the demand for Hybrid Electric Vehicles (HEV) and Electric Vehicles (EV).

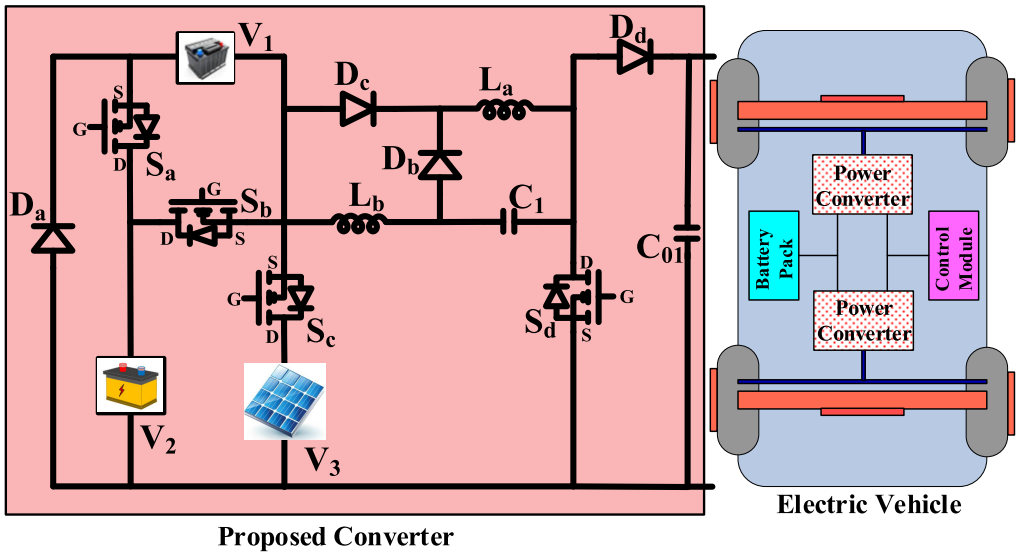

FIGURE 1. EV charging eco-system with the proposed converter.

As these vehicles become more affordable and easier to deploy, we gradually become more dependent on renewable energy sources. Photovoltaic (PV) energy is one of the most popular renewable energy sources because it requires less maintenance and offers superior efficiency, as it has no spinning or moving parts. However, PV cannot supply energy continuously as it depends on solar irradiance. A battery and ultra-capacitor are used as additional sources to meet the supply demanded by the converter. The primary purpose of deriving a multi-port DC-DC converter topology is to use it effectively for applications like Electric Vehicle (EV) charging and DC microgrid. The given converter is a multi-input converter, it can incorporate various sources, such as ultracapacitor, battery, solar-PV, etc., to deliver the necessary energy to the load. Many works have already been reported in this area.

Theoretically, a typical boost converter can achieve an unlimited voltage gain when the duty cycle value is equal to 1. However, this high-duty cycle produces high conduction loss in the active switch and diode reverse recovery loss. Additionally, the switch voltage stress is also high, which is equal to the output voltage. Isolated converters, such as forward, flyback, half-bridge, full-bridge, and push-pull types, can provide a high voltage gain by increasing the transformers' turns ratio. However, there are some challenges, such as leakage inductance and parasitic capacitance developed in the secondary winding of the transformer. This can cause high voltage and current spikes, increasing the switching devices' voltage stress.

Consequently, the power dissipation is high, increasing the switching losses and noise, further degrading the system performance [1], [2], [3], [4]. Therefore, non-isolated converters are preferred. Figure 1 shows the structure of the EV charging ecosystem with the proposed converter.

Therefore, a detailed study of the reported works is essential to understand the existing problems with the reported converter topologies. In [1], a novel non-isolated three-port DC-DC converter was proposed for low-power applications, which employed a single inductor (SI) for improved power density. However, the maximum demand control (MDC) experienced significant magnetic losses despite having fewer switching components. In [2], [3], [4], [5], and [6] is a report of an innovative MDC based on a single-inductor dual-input single-output (SI-DISO) topology. Nonetheless, the issues with ordinary single-input single-output (SISO) converters can be resolved by the recently proposed multi-port DC-DC converters (MPCs). Hence, the suggested converter can operate with high gain. In [7], a SIDO MPC was devised by incorporating buck and super-lift Luo converters, which could be used for step-up and step-down modes. However, converters with coupled inductors experience large input current ripples, which shorten the lifespan of renewable energy sources and result in conduction losses and high leakage inductances. Nevertheless, simple structures are presented in [8], [9], and [10] to avoid the drawbacks of coupled-inductor or transformer-based DC-DC boost MPCs.

The increasing demand for renewable energy sources over traditional ones is evident in the modern world [10]. However, various techniques have been proposed to ensure uninterrupted, sustainable, and sinusoidal power output from sources like batteries, photovoltaic arrays, and AC grids. In [11], different sources are fed to the controller each time to generate a suitable output compared with a reference value. A high-frequency transformer is used in [12] to isolate the source and load. Nevertheless, it causes stress across the switch to be high, which can be reduced by using non-isolated converters. To improve the reliability of using renewable energy sources, multi-port converters (MPCs) are designed

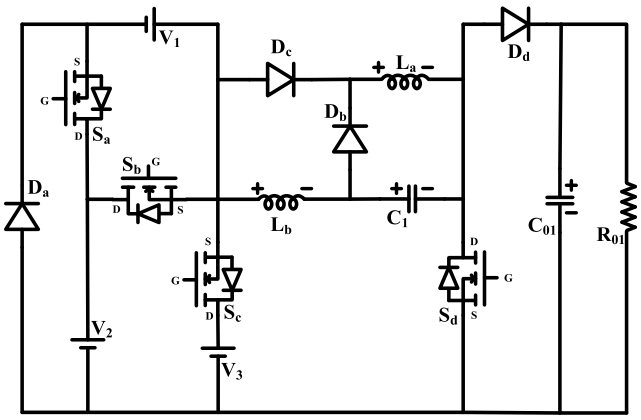

FIGURE 2. Proposed high output voltage gain FPC.

to integrate various sources [13], [14]. In [15], a primary converter with a low-power multi-port converter can extract more power from the PV load and deliver it to the output port. In [16], multiple input cells with two inductors of the same value are parallelly charged and dissipate the charged energy. These cells are integrated with conventional converters to form new topologies.

Although there have been advancements in multi-input converters, such as the novel switching mechanism based on the time-sharing method proposed in [17], several problems still need to be resolved, including multiple-inductor architectures, cross-regulation issues, and limited flexibility of regenerative loads. In many prior studies, more than one inductor is featured in the proposed converters [18], [19], [20], [21].

A simple converter can deliver two different output levels using two different sources with dissimilar voltage and current characteristics [22]. While many topologies [23], [24], [25] can meet high gain requirements, most have a longer duty cycle, posing a risk of the inductor current saturation and reducing converter performance. Extensive research has been done to develop high step-up converters that overcome the drawbacks of ordinary boost converters. As an easy technique to increase the voltage gain of the traditional boost converter, Switched Capacitor/Switched Inductor (SC/SL) Voltage Multiplier Cells (VMCs) are used [26], [27], [28]. However, in these topologies, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is connected in series with the power source at the input, which inevitably leads to pulsing input current and higher conduction losses.

In [26], SLVMCs with a two-inductor and three-diode configuration are used to create an extensible framework. The converter is equipped with two modules of SCVMCs [27], each consisting of two capacitors and two diodes. Each SL module in this arrangement is coupled to the input voltage by a MOSFET, which raises the component count overall. In [28], two MOSFETs are turned ON and OFF, and SL cells and SCVMCs are used to lessen the current strains on the switching devices. Although the topologies of the converters in [26], [27], and [28] are straightforward, using too many SC and SL modules raises costs and energy consumption.

Moreover, the input current ripple in the topologies mentioned above is significant, reducing the lifetime of the PV and FC and complicating the tracking of the maximum power point (MPPT). To address this issue, an interleaved boost converter has been proposed in [29] that features low voltage and current stress, continuous input current, and low ripple. In [30], a converter topology has been developed for highly efficient conversion with charge injection, which is suitable for a wide range of input voltages. Additionally, a converter topology has been proposed to integrate numerous sources and enhance voltage gain during bidirectional power flow [31].

In literature, various multi-input multi-output dc-dc converter topologies have been introduced with unique advantages. One topology, presented in [32], utilizes a boost converter and capacitor switching to produce different output voltage levels, regardless of input power and voltage differences. This topology offers modularity, continuous input current, and high switching frequency without a transformer. Another converter with two input sources is introduced in [33], which uses the output filter to supply the load with both input sources, making it suitable for photovoltaic systems. However, its main disadvantage is the high input current ripple. A multi-input buck dc-dc converter is also introduced in [34], capable of bidirectional power conversion and performing as a buck, boost, or buck-boost converter without requiring a transformer to generate positive output levels. Finally, the topology in [35] offers a five-port converter with internal bidirectional buck-boost capabilities, allowing for flexible connections to various sources and loads with different power and voltage requirements.

A non-isolated four-port DC-DC converter is designed to interface four power ports for hybrid energy applications, including three input ports and one output port. One of the unique features of this DC-DC converter is its use of an actively switched inductor-capacitor (ALC) network, which is not commonly found in other multi-port converters. This allows the converter to achieve a high output voltage gain of 4.75, significantly higher than what other multi-port converters in the literature have achieved. Moreover, it achieved a high efficiency of 96.77% and minimized the component count by reducing the number of switches per input port. This converter operates in five modes, with the switching patterns easily alterable to interface all sources and either with the load. A complete switch voltage stress (VS) analysis of the converter, describing the circuit topology, modes of operation, and presenting simulation and real-time validations. In summary, the non-isolated four-port DC-DC converter for hybrid energy applications offers unique features that distinguish it from other multi-port converters in the literature. Its high output voltage gain, high efficiency, and minimized component count make it particularly suitable for use in hybrid energy applications like fast charging of electric vehicles.

This work proposes a new FPC converter topology with several advantages, including high output voltage gain, low voltage stress, and high efficiency. The proposed topology has improved working modes, leading to better performance. The paper is structured as follows: Section II details the proposed FPC circuit, its mode, and analytical operation. Section IV presents the steady-state simulation results and their descriptions. Section V discusses the hardware realization experimentation and results. Finally, Section VI presents the conclusion.

III. PROPOSED TOPOLOGY

The topology for the proposed FPC is depicted in Fig. 2. The proposed converter consists of three input ports V_1(Ultra-capacitor), V_2 (Battery), and V_3 (PV). S_a, S_b, S_c, and S_d are the four power switches. It employs four power diodes D_a, D_b, D_c, and D_d, which ensure the correct freewheeling path for the current during various modes of operation. The passive elements utilized in the topology comprise two inductors L_a and L_b, two capacitors C_1 and C_{01} and a resistor R_{01} acting as load. Inductor L_a, L_b and capacitor C_1 constitute and responsible for the proposed converter's desired high output voltage gain. Capacitor C_{01} finds its application in supplying the load whenever it is isolated during different modes of operation. The modes of operation and the respective equivalent circuits are discussed in the following section.

A. MODES OF OPERATION

This section deals with the various modes of operation of the proposed converter. In the following equivalent circuit for each mode, inductor voltage equations and capacitor current equations are also described for the ideal case. These equations will be further employed for the lossless converter steady-state analysis.

1) MODE I

Mode-I begins at t = 0, when switches S_a and S_d are turned ON, as illustrated in Fig. 3(a), and its equivalent circuit for this mode is shown in Fig. 3. In this mode, sources V_1 and V_2 act in series to charge inductors L_a and L_b. Capacitor C_{01} supplies the load. This mode persists till $t = \alpha_1 T$, where T is the converter operating time period, determined by the frequency of operation. Capacitor C1 is charging with the support of sources V1 and V2. The steady-state inductor voltage and capacitor current equations are developed as follows.

For Inductor voltage L_a:

$$V_{L_a} = V_1 + V_2 \tag{1}$$

For Inductor voltage L_b:

$$V_{L_b} = V_1 + V_2 + V_{C_1} \tag{2}$$

For Capacitor current I_{C_1}:

$$I_{C_1} = I_{L_b} \tag{3}$$

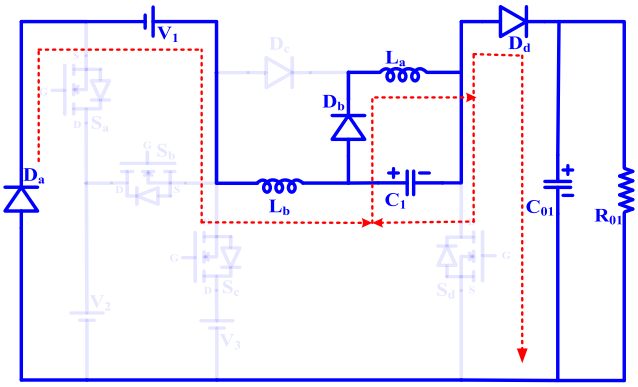

FIGURE 3. Modes of operation of the proposed converter. (a) Mode I (b) Mode II, (c) Mode III, (d) Mode IV and (e) Mode V.

For Capacitor current $I_{C_{01}}$:

$$I_{C_{01}} = -I_0 \tag{4}$$

2) MODE II

In this mode, switches S_b and S_d are turned ON, and the equivalent circuit of this mode is shown in Fig. 3(b). Source V_2 charges the inductors L_a and L_b along with C_1, and C_{01} feeds the load. This mode begins at $t = \alpha_1 T$ and ends at $t = (\alpha_1 + \alpha_2)$ T. The inductor voltage and capacitor equations are formulated below.

For Inductor voltage L_a:

$$V_{L_a} = V_2 \tag{5}$$

For Inductor voltage L_b:

$$V_{L_b} = V_2 + V_{C_1} \tag{6}$$

For Capacitor current I_{C_1}:

$$I_{C_1} = I_{L_b} \tag{7}$$

For Capacitor current $I_{C_{01}}$:

$$I_{C_{01}} = -I_0 \tag{8}$$

3) MODE III

Fig. 3(c) shows the equivalent circuit of mode III. This mode commences at $t = (\alpha_1 + \alpha_2)T$, when switch S_c is turned ON, and switch S_d continues to be in ON state from the previous mode. Here, source V_3 charges inductors L_a and L_b together with C_1. C_{01} supplies the load. Anti-parallel diode in switch S_c will be forward bias in modes 1, mode2, 4, and 5. However, in mode 3, the switch S_c is conducting, which makes the anti-parallel diode to be in reverse bias. Thus, the anti-parallel diode across S_c will be reverse bias in this mode. This mode ends at $t = (\alpha_1 + \alpha_2 + \alpha_3)T$, and the inductor voltage and capacitor current equations are written below.

For Inductor voltage L_a:

$$V_{L_a} = V_3 \tag{9}$$

TABLE 1. Component current stress and loss break down.

S.No.	Element	RMS Current	Loss Expression	Total Loss
1.	L_a	$I_{La} = \frac{I_o}{(1-\alpha_4)^2}$	$I_{La}^2 R_L$	$P_{Loss} = (I_{La}^2 + I_{Lb}^2)R_L$
2.	L_b	$I_{Lb} = \frac{I_o}{(1-\alpha_4)}$	$I_{Lb}^2 R_L$	
3.	S_a	$I_{Sa} = (I_{La} + I_{Lb})\sqrt{\alpha_1}$	$I_{Sa}^2 R_{ON}$	$P_{Loss} = (I_{Sa}^2 + I_{Sb}^2 + I_{Sc}^2 + I_{Sd}^2)R_{ON}$
4.	S_b	$I_{Sb} = (I_{La} + I_{Lb})\sqrt{\alpha_2}$	$I_{Sb}^2 R_{ON}$	
5.	S_c	$I_{Sc} = (I_{La} + I_{Lb})\sqrt{\alpha_3}$	$I_{Sc}^2 R_{ON}$	
6.	S_d	$I_{Sd} = (I_{La} + I_{Lb})\sqrt{\alpha_4}$	$I_{Sd}^2 R_{ON}$	
7.	D_a	$I_{Da} = \sqrt{(1-\alpha_3-\alpha_2-\alpha_1)}I_{La} + \sqrt{(\alpha_4-\alpha_3-\alpha_2-\alpha_1)}I_{Lb}$	$I_{Da}^2 R_D$	$P_{Loss} = (I_{Da}^2 + I_{Db}^2 + I_{Dc}^2 + I_{Dd}^2)R_D$
8.	D_b	$I_{Db} = \sqrt{(1-\alpha_4)}I_{La}$	$I_{Db}^2 R_D$	
9.	D_c	$I_{Dc} = \sqrt{\alpha_4}I_{La}$	$I_{Dc}^2 R_D$	
10.	D_d	$I_{Dd} = \sqrt{(1-\alpha_4)}I_{La}$	$I_{Dd}^2 R_D$	

For Inductor voltage L_b:

$$V_{L_b} = V_3 + V_{C_1} \tag{10}$$

For Capacitor current I_{C_1}:

$$I_{C_1} = I_{L_b} \tag{11}$$

For Capacitor current $I_{C_{01}}$:

$$I_{C_{01}} = -I_0 \tag{12}$$

4) MODE IV

In this mode, only S_d remains ON, rest all other switches are turned OFF. The equivalent circuit for this mode is displayed in Fig. 3(d). Here, V_1 charges inductors L_a and L_b together with C_1. This is the last mode in which inductors are charged continuously. This mode starts at $t = (\alpha_1 + \alpha_2 + \alpha_3)$ T and lasts till α_4T, C01 supplies the load. The inductor voltages and capacitor current equations are developed below.

For Inductor voltage L_a:

$$V_{L_a} = V_1 \tag{13}$$

For Inductor voltage L_b:

$$V_{L_b} = V_1 + V_{C_1} \tag{14}$$

For Capacitor current I_{C_1}:

$$I_{C_1} = I_{L_b} \tag{15}$$

For Capacitor current $I_{C_{01}}$:

$$I_{C_{01}} = -I_0 \tag{16}$$

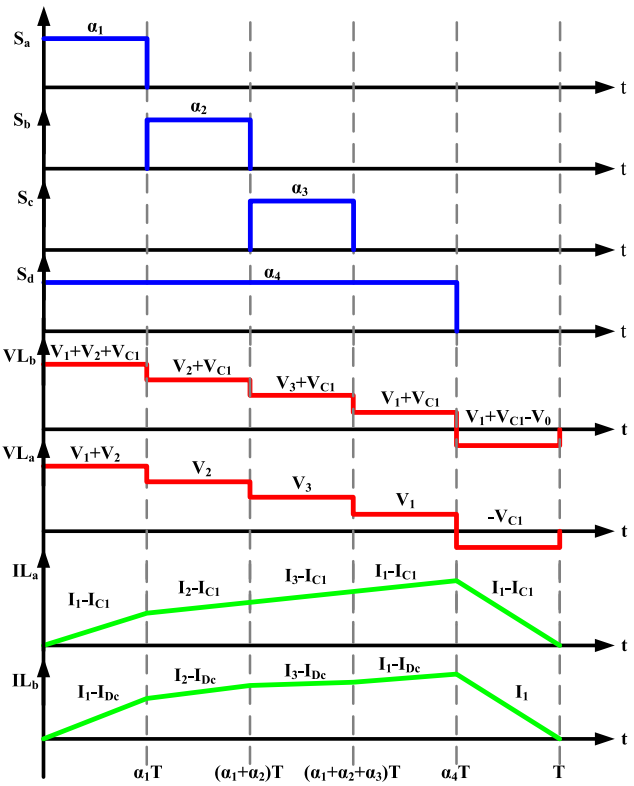

FIGURE 4. Analytical waveforms of proposed converter.

5) MODE V

This is the last mode of converter operation, and the corresponding circuit structure is illustrated in Fig. 3(e). In this mode, all the switches are turned OFF and the load is

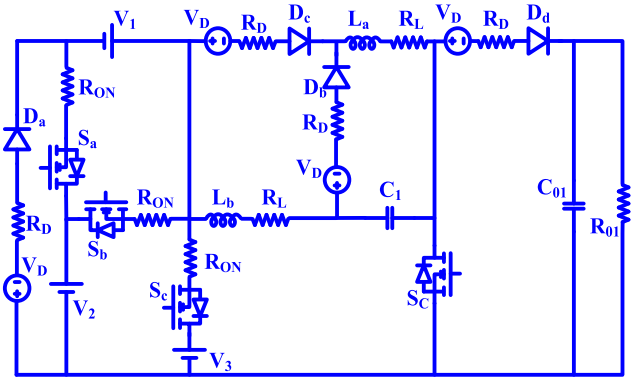

FIGURE 5. Converter topology of non-ideal case depicting various losses.

connected via diode D_d. Inductors L_a and L_b act in series with source V_1 and supply to the load. The continuous charging of the inductors and their series coupled arrangement while discharging in this mode are responsible for the high output voltage of the proposed converter. Also, capacitor C_1 is replenished by L_a. This mode begins at $t = \alpha_4 T$ and works till the end of one complete cycle. The inductor L_a is charging with the support of discharging the capacitor C_1 which helps improve the converter's gain. The inductor voltage and capacitor current equations for this mode are as follows.

For Inductor voltage L_a:

$$V_{L_a} = -V_{C_1} \tag{17}$$

For Inductor voltage L_b:

$$V_{L_b} = V_1 + V_{C_1} - V_0 \tag{18}$$

For Capacitor current I_{C_1}:

$$I_{C_1} = I_{L_b} = I_{L_a} \tag{19}$$

For Capacitor current $I_{C_{01}}$:

$$I_{C_{01}} = I_{L_b} - I_0 \tag{20}$$

B. ANALYTICAL OPERATION

Analytical waveforms of inductor voltage, inductor currents, and switch pulse of S_a, S_b, S_c and S_d are indicated in Fig.4. S_a is triggered for a duration of $\alpha_1 T$ at $t = 0$. Then S_b is triggered at $t = \alpha_1 T$ for a duration of $\alpha_2 T$. After S_b, S_c is operated for a period of $\alpha_3 T$. Switch S_d is triggered at $t = 0$ with S_a and it remains ON for a period of $\alpha_4 T$. For the remaining time period, all switches are turned OFF. The switches Sa, S_b, and S_c have duty ratios of α_1, α_2, and α_3 is 20%, and switch S_d has a duty ratio of $\alpha 4$ is 70%. The waveforms for both the inductor voltages have five voltage levels, four charging modes and one discharging mode. These waveforms are constructed using steady-state inductor voltage equations. The inductors charge to different voltage levels corresponding to each mode and then discharge in fifth mode. Similar to the inductor voltage waveforms, the analytical inductor current waveforms are obtained from the inductor voltage equation under each mode of operation. The current through both inductors increase in mode I, where they are charged with maximum voltage. The inductor currents continue to increase in modes II and III, but with a lesser slope due to decreased charging voltage. The current reaches their peak in mode IV, after which the current is decreases inductors begin to discharge.

IV. STEADY STATE ANALYSIS

This section presents a steady-state analysis of the proposed FPC. The investigation is performed for both ideal and non-ideal cases. In non-ideal cases, parasitic losses are considered. Parameters are calculated and include the output voltage expression and inductor current expression in terms of load current for the ideal case. In contrast, losses due to each passive element are included in the non-ideal case.

A. IDEAL CASE

The expression for the ideal output voltage can be calculated using the principles of inductor volt-sec balance and capacitor amp-sec balance. Applying volt-sec balance for L_a, from equations (1), (5), (9), (13), and (17).

$$\alpha_1 (V_1 + V_2) + \alpha_2 V_2 + \alpha_3 V_3 + (\alpha_4 - \alpha_3 - \alpha_2 - \alpha_1) V_1 - (1-\alpha_4) V_{C1} = 0 \tag{21}$$

Solving for V_{C1},

$$V_{C1} = \frac{(\alpha_4 - \alpha_3 - \alpha_2) V_1 + (\alpha_1 + \alpha_2) V_2 + \alpha_3 V_3}{(1 - \alpha_4)} \tag{22}$$

Similarly, applying volt-sec balance for inductor L_b, from equations (2), (6), (10), (14), and (18).

$$\alpha_1 (V_1 + V_2 + V_{C1}) + \alpha_2 (V_2 + V_{C1}) + \alpha_3 (V_3 + V_{C1}) + \alpha_4 (V_1 + V_{C1}) + (1 - \alpha_4) (V_1 + V_{C1} + V_o) = 0 \tag{23}$$

$$(1 - \alpha_3 - \alpha_2) V_1 + (\alpha_1 + \alpha_2) V_2 + \alpha_3 V_3 + V_{C1} = (1 - \alpha_4) V_o \tag{24}$$

Substituting equation (22) in (24), the expression for the ideal output voltage is obtained (25), as shown at the bottom of the next page.

The proposed DC-DC converter is designed for EV charging applications requiring more current than voltage. This converter aims to achieve a voltage gain of 5 times. Existing literature works achieve this voltage gain using transformers and voltage multipliers. In contrast, our proposed converter achieves a voltage gain of 4.5 times without using a transformer or voltage multiplier, representing a significant improvement. Additionally, the voltage gain is achieved with a duty cycle of only 20%, which means further enhancement can be achieved by adjusting the duty cycle.

B. NON-IDEAL CASE

Fig. 5 depicts the topology of the proposed converter in a non-ideal case. Here each component is modeled with its possible source of losses. The various parasitic elements are modeled

TABLE 2. Component comparison with other converters.

Parameters	[18]	[24]	[26]	[29]	[30]	[31]	Proposed
Inductors count	4	4	8	6	4	4	2
Switches count	4	1	4	12	2	5	4
Diodes count	7	3	16	-	9	1	4
Capacitor count	7	6	1	2	6	4	2
Output Voltage	$V_o = \frac{m}{1-d}$	$V_o = \frac{3DV_i}{1-D}$	$V_o = \frac{1+(2n+3)D}{1-D}$	$V_o = \frac{1+n+d}{(1-d)^2}$	$V_o = \frac{4}{1-d}$	$V_o = \frac{(d_1-2d_2+d_1d_2)}{(1-d_1)^2(d_1-d_2)}V_1 + \frac{d_2(1-d_1)}{d_1(d_1-d_2)}V_2$	$V_o = \frac{[1+(\alpha_2+\alpha_3)(\alpha_4-2)]V_1+(2-\alpha_4)[(\alpha_1+\alpha_2)V_2+\alpha_3V_3]}{(1-\alpha_4)^2}$
Voltage stress	$\frac{V_o}{m}$	$\frac{V_o}{3D}$	$\frac{V_o[(n+1)+M]}{(n+2)M}$	$\frac{V_o}{1+n+d}$	$\frac{2V_{in}}{1-d}$	$V_o - \left(\frac{d_1}{d_1-d_2-d_1^2}\right) * \left(V_2 - \frac{d_1}{(1-d_1)}\right)$	$V_o(1-\alpha_4) + V_1(3\alpha_2-1) + V_2(2-\alpha_1+3\alpha_2) + V_3(1-2\alpha_3)$
Efficiency	96	93.3	95.6	92	94	95	96.7
Total number of devices	22	14	29	20	21	14	12

as follows. The parasitic winding resistance R_L and parasitic on-state resistance R_{ON}, are in series to the inductors and power switches, respectively. Similarly, voltage source V_D and resistance R_D are the parasitic elements existing in series to diodes. This circuit is employed for the loss and efficiency analysis of the proposed converter.

The loss expression for an element is given by:

$$P_{Loss} = I_{RMS}^2 R \tag{26}$$

The above equation is used for the loss analysis of various passive elements in the proposed topology. I_{RMS} is the rms current through the element and R is the effective resistance are shown in (26). Table 1 states that rms current through all the switches, diodes and inductors, and losses occurring in each element are obtained and further employed efficiency analysis of the present converter. The expression for converter efficiency is formulated as follows.

The total power loss occurring in the inductors is described by equation (27).

$$P_{Loss} = (I_{La}^2 + I_{Lb}^2)R_L \tag{27}$$

Similarly, the respective losses due to the switches and diodes are specified in equations (28) and (29), respectively.

$$P_{Loss} = (I_{Sa}^2 + I_{Sb}^2 + I_{Sc}^2 + I_{Sd}^2)R_{ON} \tag{28}$$

$$P_{Loss} = (I_{Da}^2 + I_{Db}^2 + I_{Dc}^2 + I_{Dd}^2)R_D \tag{29}$$

The power loss of each part of inductor, switch, and diode loss has been calculated from the formula listed in Table 1.

Now, the converter efficiency (η) is described as follows.

$$\eta = \frac{\text{Output}}{\text{Output} + \text{Losses}}$$

The converter output is V_oI_o, where V_o is the load voltage and I_o is the load current. The total losses are the sum of all the three losses which are described by equations (27), (28) and (29). Therefore, the converter efficiency is formulated in equation (30), as shown at the bottom of the next page.

Inductor design: The inductor is designed using the inductor charging-discharging cycle and the inductor current peak to peak ripple [21]. For this purpose, the peak-to-peak ripple is considered as 10% of the load current. Therefore, during the charging cycle of the inductor, the peak-to-peak ripple is expressed as follows.

For inductor L_a, (31), as shown at the bottom of the next page.

So, equation (32) yields the value of L_a

$$L_a = \frac{V_2(\alpha_1+\alpha_2) + V_3\alpha_3 + V_1(\alpha_4-\alpha_3-\alpha_2)}{f\Delta i_{L_a}} \tag{32}$$

For inductor L_b, (33) , as shown at the bottom of the next page.

So, equation (34) yields the value of L_b

$$L_b = \frac{V_2(\alpha_1+\alpha_2) + V_3\alpha_3 + V_1(\alpha_4-\alpha_3-\alpha_2) + \alpha_4V_{C1}}{f\Delta i_{L_b}} \tag{34}$$

$$V_o = \frac{[1+(\alpha_2+\alpha_3)(\alpha_4-2)]V_1 + (2-\alpha_4)[(\alpha_1+\alpha_2)V_2 + \alpha_3V_3]}{(1-\alpha_4)^2} \tag{25}$$

TABLE 3. Voltage stress across switches and diodes of the proposed FPC.

S. No.	Component	Mode I	Mode II	Mode III	Mode IV	Mode V	Average voltage stress
1.	S_a	0	V_1	$V_2 - V_1$	V_2	V_2	$(1-\alpha_1)V_2 + \alpha_2(V_1 - V_2) - \alpha_3 V_1$
2.	S_b	$-V_1$	0	$V_2 - V_3$	$V_2 - V_1$	$V_2 - V_1$	$\alpha_1 V_2 + (1-\alpha_2)(V_2 - V_1) + \alpha_3(V_1 - V_3)$
3.	S_c	$V_3 - V_2 - V_1$	$V_3 - V_2$	0	$V_3 - V_1$	$V_3 - V_1$	$-\alpha_1 V_2 + \alpha_2(V_1 - V_2) + (1-\alpha_3)(V_3 - V_1)$
4.	S_d	0	0	0	0	V_o	$(1-\alpha_4)V_o$
5.	D_a	$-V_2$	$V_1 - V_2$	$V_1 - V_3$	0	0	$-\alpha_1 V_2 + \alpha_2(V_1 - V_2) + \alpha_3(V_1 - V_3)$
6.	D_b	$-(V_1 + V_2 + V_{C1})$	$-(V_2 + V_{C1})$	$-(V_3 + V_{C1})$	$-(V_1 + V_{C1})$	0	$-\alpha_1 V_2 + \alpha_2(V_1 - V_2) + \alpha_3(V_1 - V_3) - \alpha_4(V_1 + V_{C1})$
7.	D_c	0	0	0	0	$V_1 + V_{C1} - V_o$	$(1-\alpha_4)(V_1 + V_{C1} - V_o)$
8.	D_d	$-V_o$	$-V_o$	$-V_o$	$-V_o$	0	$-\alpha_4 V_o$

TABLE 4. Simulation parameters.

S. No.	Parameter	Specification
1.	Input Voltage (V_1)	12 V
2.	Input Voltage (V_2)	36 V
3.	Input Voltage (V_3)	24 V
4.	Inductor ($L_a = L_b$)	5 mH
5.	Capacitor ($C_1 = C_{01}$)	100 µF
6.	Load Resistor (R_0)	300 Ω
7.	Switching Frequency	20kHz

The comparison of components counts, voltage gain, voltage stress, and efficiency with other converters has been described in Table 2. The voltage stresses across the switches and diodes are presented in Table 3 for various operation modes.

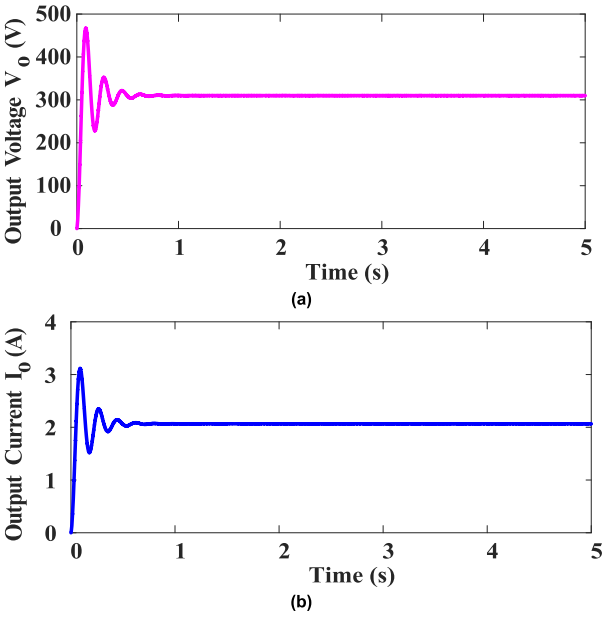

FIGURE 6. Simulation waveform of (a) output voltage, (b) Output current.

V. SIMULATION RESULTS AND DISCUSSION

A. STEADY STATE RESULTS

The proposed FPC is simulated in MATLAB/Simulink software. The analysis of voltage stress across the switches and diodes are presented. The respective current stresses have been shown in Table 1, under the previous section. The

$$\eta = \frac{V_o I_o}{V_o I_o + \left(I_{La}^2 + I_{Lb}^2\right) R_L + \left(I_{Sa}^2 + I_{Sb}^2 + I_{Sc}^2 + I_{Sd}^2\right) R_{ON} + \left(I_{Da}^2 + I_{Db}^2 + I_{Dc}^2 + I_{Dd}^2\right) R_D} \tag{30}$$

$$\Delta i_{L_a} = \frac{(V_1 + V_2)\,\alpha_1 + V_2\alpha_2 + V_3\alpha_3 + V_1(\alpha_4 - \alpha_3 - \alpha_2 - \alpha_1)}{f L_a} \tag{31}$$

$$\Delta i_{L_b} = \frac{(V_1 + V_2 + V_{C1})\,\alpha_1 + (V_2 + V_{C1})\alpha_2 + (V_3 + V_{C1})\alpha_3 + (V_1 + V_{C1})(\alpha_4 - \alpha_3 - \alpha_2 - \alpha_1)}{f L_b} \tag{33}$$

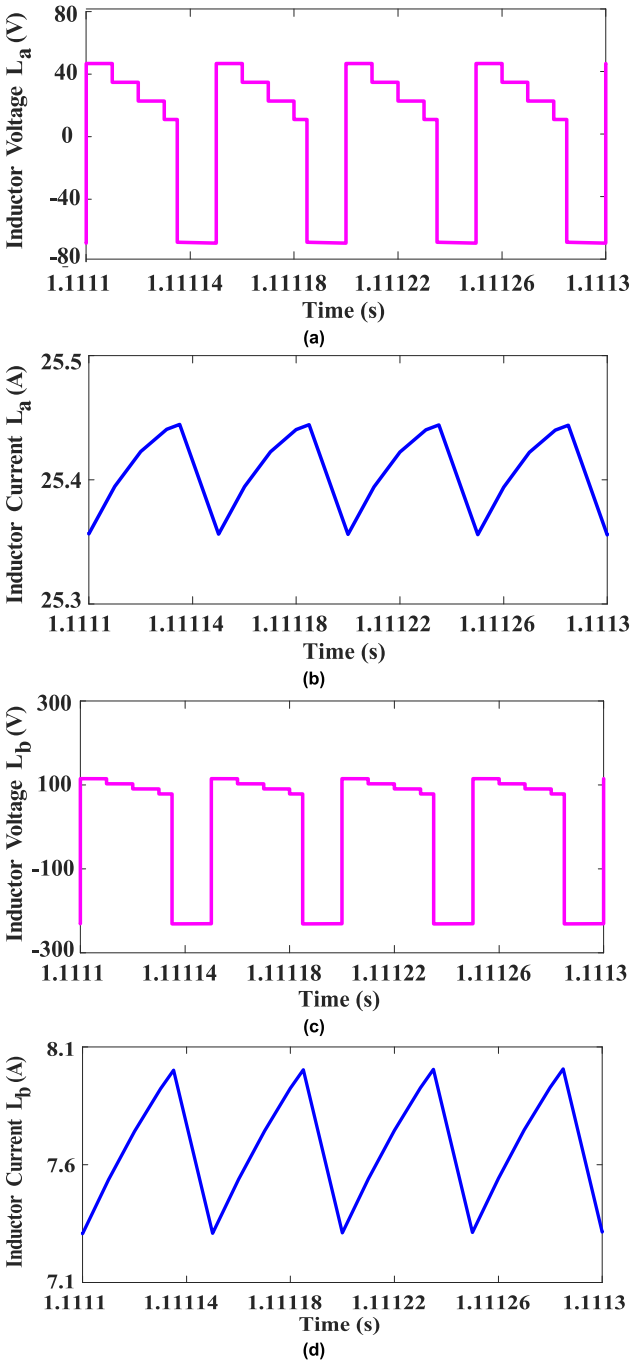

FIGURE 7. Simulation waveforms of (a) Inductor voltage (L_a), (b) Inductor current (L_a), (c) Inductor voltage (L_b), (d) Inductor current (L_b).

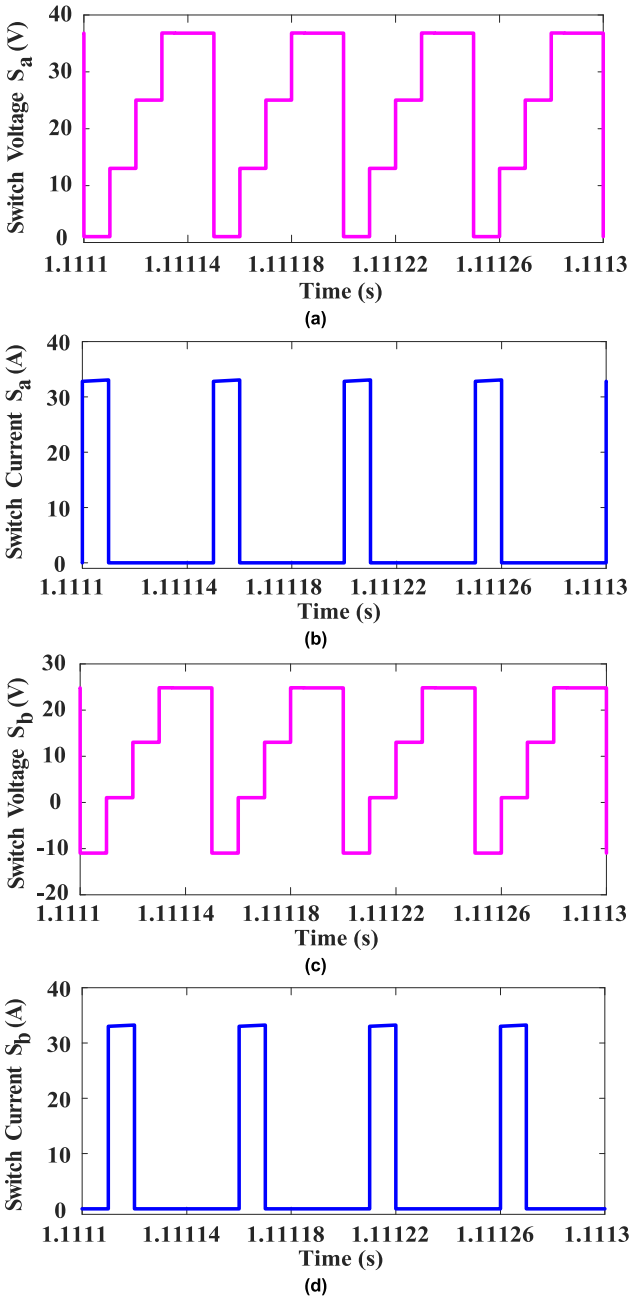

FIGURE 8. Simulation waveforms of (a) Switch voltage (S_a), (b) Switch current (S_a), (c) Switch voltage (S_b), (d) Switch current (S_b).

simulation parameters for the proposed FPC are described in Table 4. The ideal and non-ideal case of steady-state analysis is given in section III.

Fig. 6 portrays load voltage and current waveforms. The load voltage stabilizes at a steady-state value of 310 V, to achieve this 12 V, 24 V, and 36 V sources voltages are used. The current drawn by the load settles to a value of 2 A, since a resistive load of 300 Ω is employed, yielding a voltage gain of 4.75 times of input voltage.

The comparison of components counts, voltage gain, voltage stress, and efficiency with other converters has been described in Table 2. The voltage and current waveforms for inductors L_a and L_b are represented in Fig. 7. It is evident from the figures that the waveforms are identical to the analytical waveforms depicted in Fig. 4. Inductor L_a charges to 48 V (V_1+V_2) in mode I, 36 V (V_2) in mode II, 24 V (V_3) in mode III, 12 V (V_1) in mode IV. Finally, it discharges to -70 V during mode V. Similarly; Inductor L_b is charged to a higher voltage as it is in series with capacitor C_1. Consequently, it is charged to 115 V (V_1+V_2+V_{C1}) in mode I,

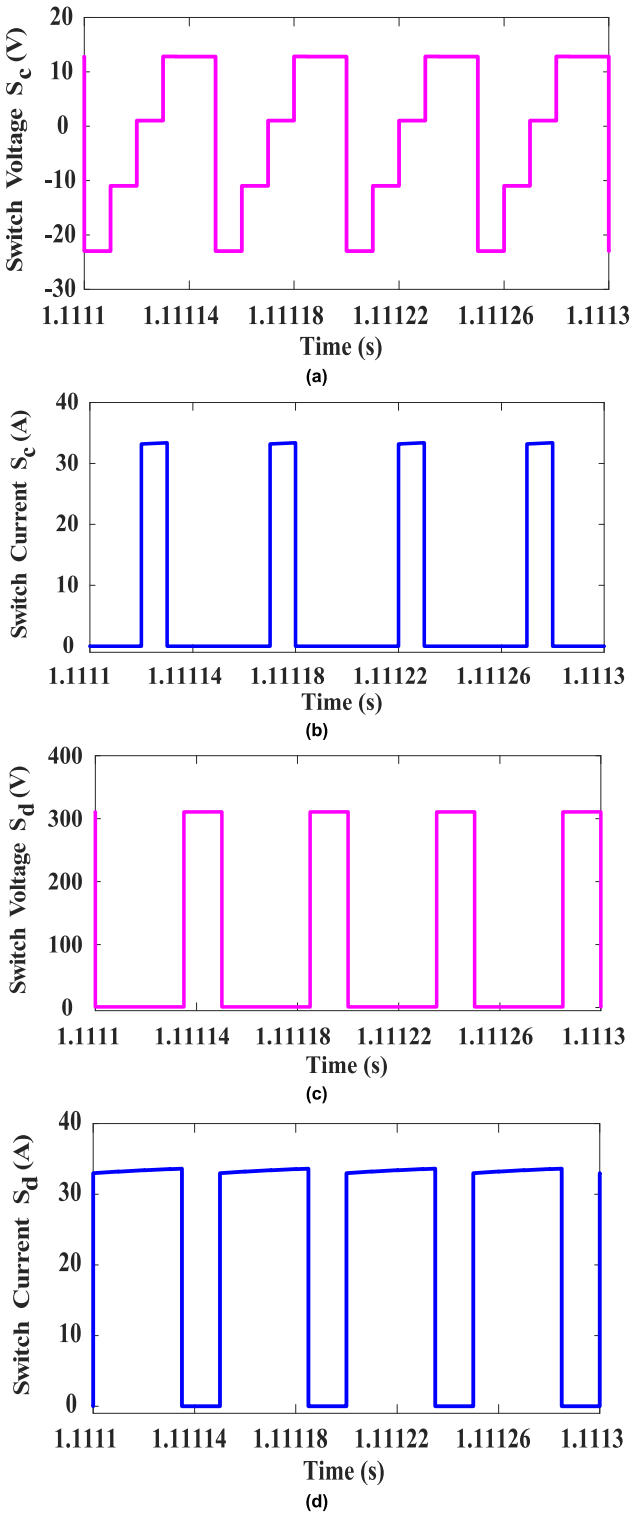

FIGURE 9. Simulation waveforms of (a) Switch voltage (S_c), (b) Switch current (S_c), (c) Switch voltage (S_d), (d) Switch current (S_d).

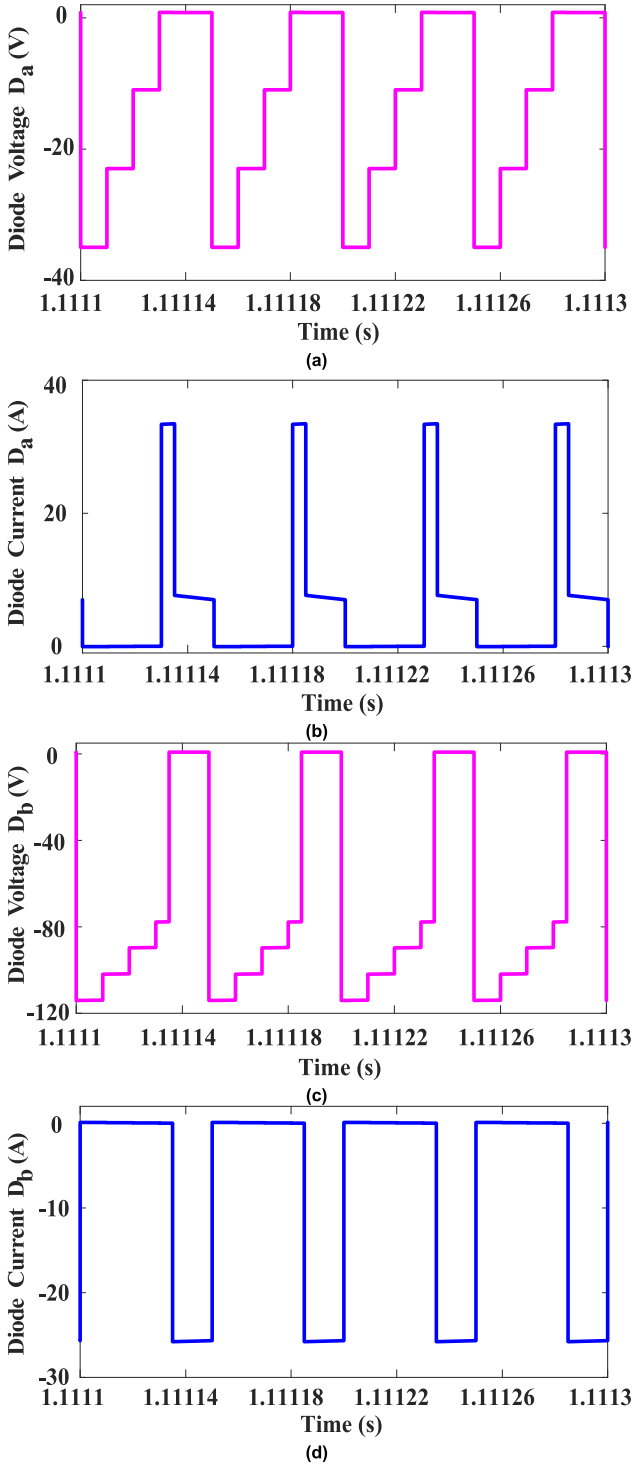

FIGURE 10. Simulation waveforms of (a) Diode voltage (D_a), (b) Diode current (D_a), (c) Diode voltage (D_b), (d) Diode current (D_b).

102 V ($V_2 + V_{C1}$) in mode II, 90 V (V_3+V_{C1}) in mode III, 78 V ($V_1 + V_{C1}$) in mode IV, and discharges to -231 V ($V_1 + V_{C1} - V_o$) during mode V. This series discharging of inductors L_a and L_b is responsible for the high output voltage capability of the proposed FPC. The current through L_a attains a peak value of 24.45 A and the lowest value of 23.35 A resulting in a peak-to-peak ripple of 0.1 A. The maximum value attained by current through L_b is 8 A and minimum value of 7.3 A yielding a peak-to-peak ripple of 0.7 A.

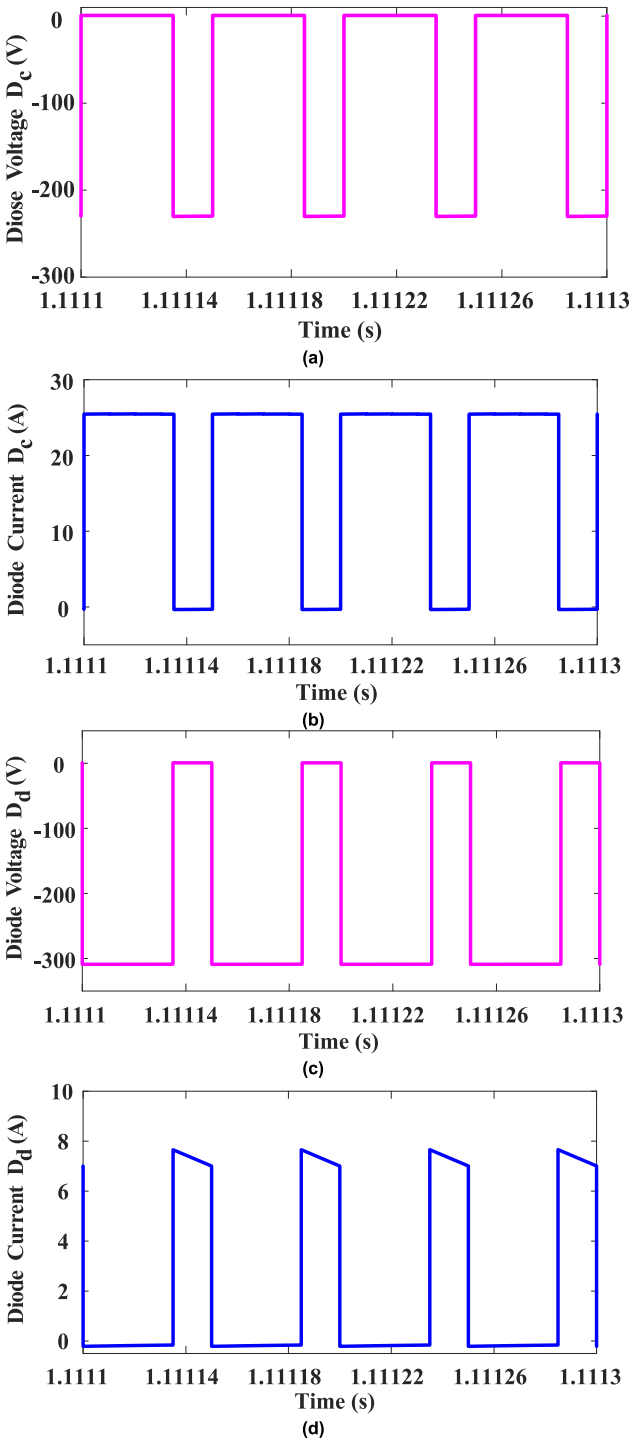

FIGURE 11. Simulation waveforms of (a) Diode voltage (D_c), (b) Diode current (D_c), (c) Diode voltage (D_d), (d) Diode current (D_d).

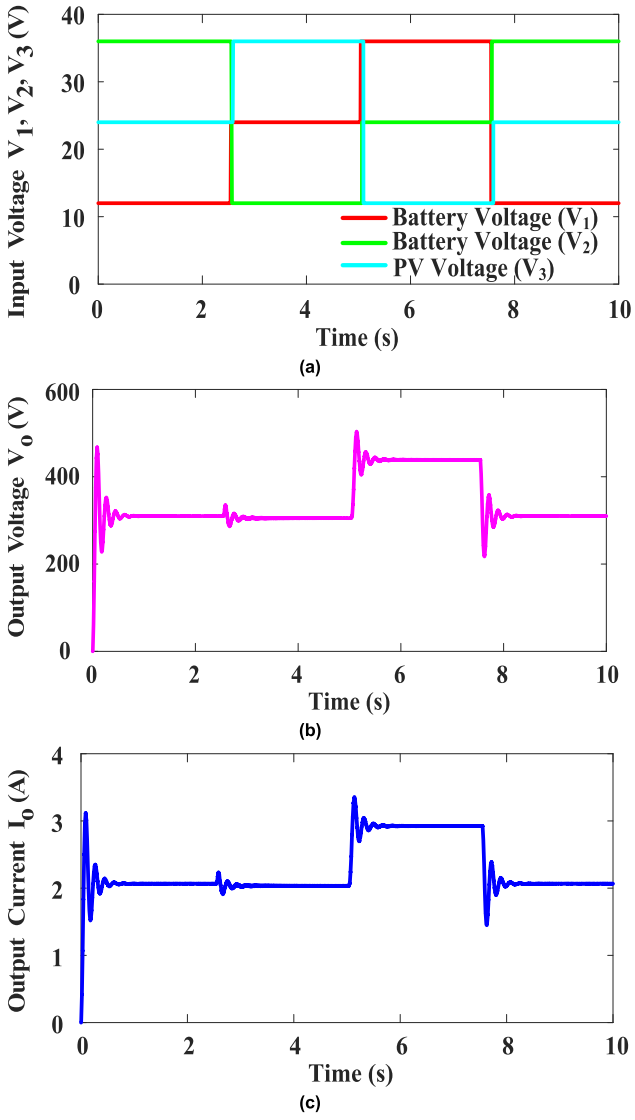

FIGURE 12. Simulation waveforms of step variation in input supply voltage.

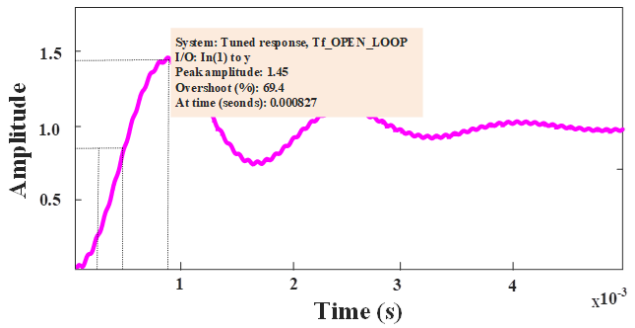

FIGURE 13. Step response for proposed converter in open loop system.

Fig.8 and 9 depicts the voltage and current waveforms for switches S_a, S_b, S_c, and S_d, respectively. Table 3 presents the voltage stresses across the switches during various modes of operation. For the sake of simplicity, the switch voltage drop is ignored in the voltage stress analysis. Fig. 8 depicts the voltage stress across S_a during mode I is 0, as it conducts. The stress rises to 12 V (V_1) in mode II, further increasing 24 V (V_2-V_1) in mode III and remains at a constant value of 36 V (V_2) during mode IV and V.S_b is exposed to -12 V ($-V_1$) in mode I, no stress during mode II, 12 V (V_2-V_3) in mode III

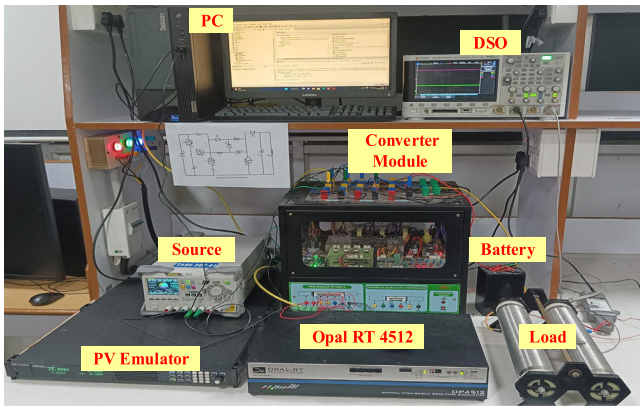

FIGURE 14. Converter topology of experimental setup.

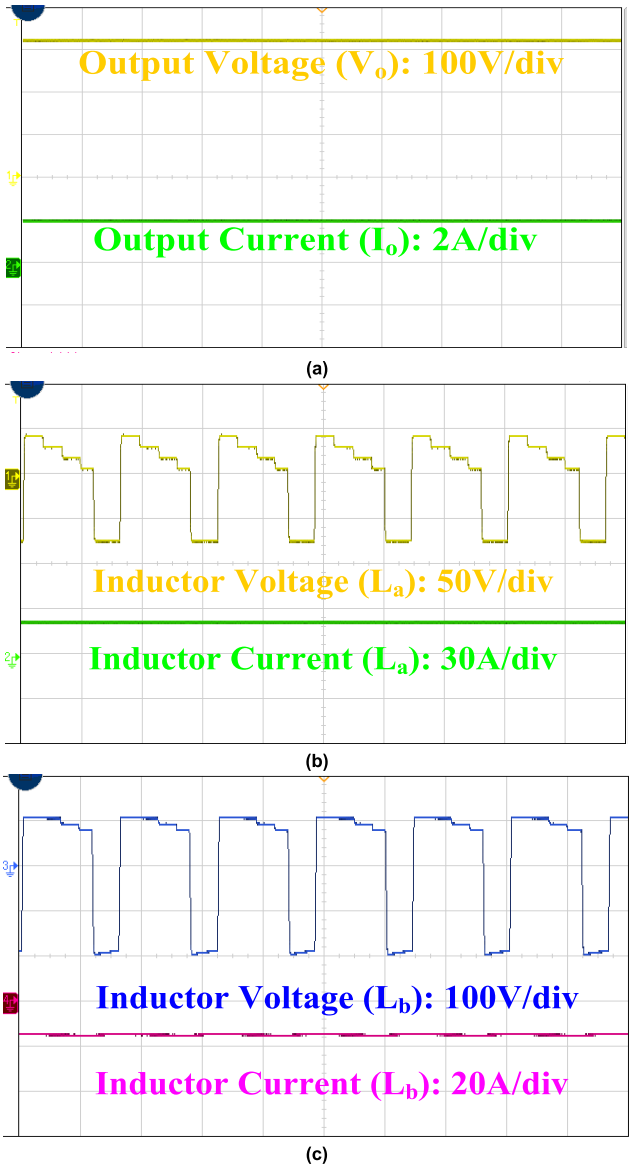

FIGURE 15. Simulation waveforms of step variation in input supply voltage.

and 24 V (V_2-V_1) in mode IV and V. Fig. 9 depicts the voltage stress across S_c, during mode I -24 V ($V_2-V_1-V_3$), -12 V (V_3-V_2) in mode II, 0 V during mode III and 12 V (V_3-V_1) throughout mode IV and V. In Switch S_d, there is no voltage stress for first four modes and 300 V (V_o) appears across S_d during mode V. The average voltage stress across all the switches for one cycle of converter operation is presented in Table 3 and the rms currents through each switch are presented in Table 1.

TABLE 5. Electrical Specification for experimental parameters.

S. No.	Parameter	Specification
1.	Ultracapacitor Voltage (V_1)	12 V
2.	Battery Voltage (V_2)	36 V
3.	PV Voltage (V_3)	24 V
4.	Inductor ($L_a = L_b$)	5 mH
5.	Capacitor ($C_1 = C_{01}$)	100 µF, 450V
6.	Load Resistor (R_0)	300 Ω
7.	Switching Frequency	20kHz
8.	Opal RT	OP4512
9.	MOSFET	600V, 20A
10.	Diode	600V, 30A
11.	DSO (Keysight)	Infinii Vision DSOX3034T
12.	Output Voltage (Vo)	310V
13.	Output Power (W)	600W

Fig. 10 and 11 depicts the voltage and current waveforms for diodes D_a, D_b, D_c and D_d respectively. The voltage stress for all five modes and average stress across the diodes for entire converter operation is represented in Table 3, the rms current through each diode is depicted in Table 1. D_a is exposed to a voltage stress of -36 V ($-V_2$) during mode I, -24 V (V_1-V_2) in mode II, -12 V (V_1-V_3) in mode III and 0 V in mode IV and V. Diode D_b as a voltage stress of -115 V ($-V_{C1}-V_1-V_2$) in mode I, -102 V ($-V_{C1}-V_2$) in mode II, -90 V ($-V_{C1}-V_3$) in mode III, -78 V ($-V_{C1}-V_1$) in mode IV and 0 V in mode V. As D_c conducts for the first four modes and voltage stress of -231 V ($V_1 + V_{C1} - V_o$) in mode V.

The voltage stress of -300 V ($-V_o$) appears across D_d for the first four modes, and in the fifth mode it is conducting since no voltage stress across it.

B. DYNAMIC STATE RESULTS

To test the dynamic response of converter topology with open loop control, source voltage variations and output disturbances are executed. Fig.12 shows step variation implemented to the input supply voltage V_1 from 12V to 24V, then further increased to 36V, V_2 is varied simultaneously from 36V to 12V followed by 24V, and V_3 is changed from 24V to 36V, then to 12V at the same period. It is observed that the output voltage of the converter settles to 310V with irrespective of supply voltage variations. Correspondingly, a dynamic step change in load is performed at the output side of the converter as shown in Fig.12.

The proposed topology's stability analysis considers the values of the inductors L_a and L_b and the capacitors C_1

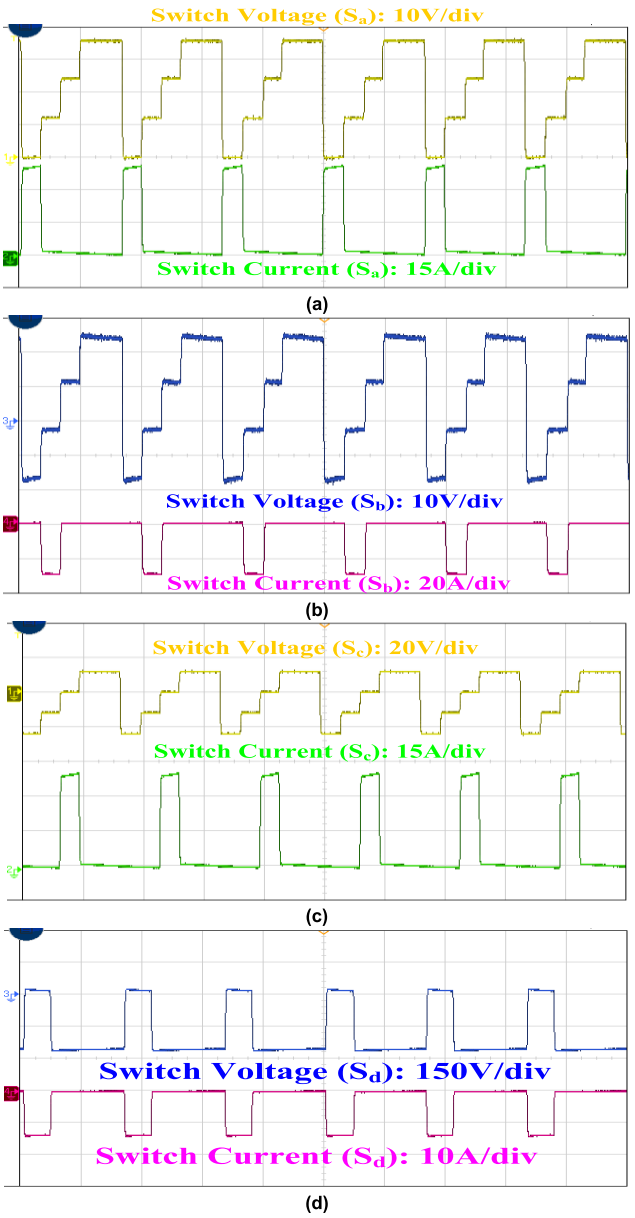

FIGURE 16. Simulation waveforms of step variation in input supply voltage.

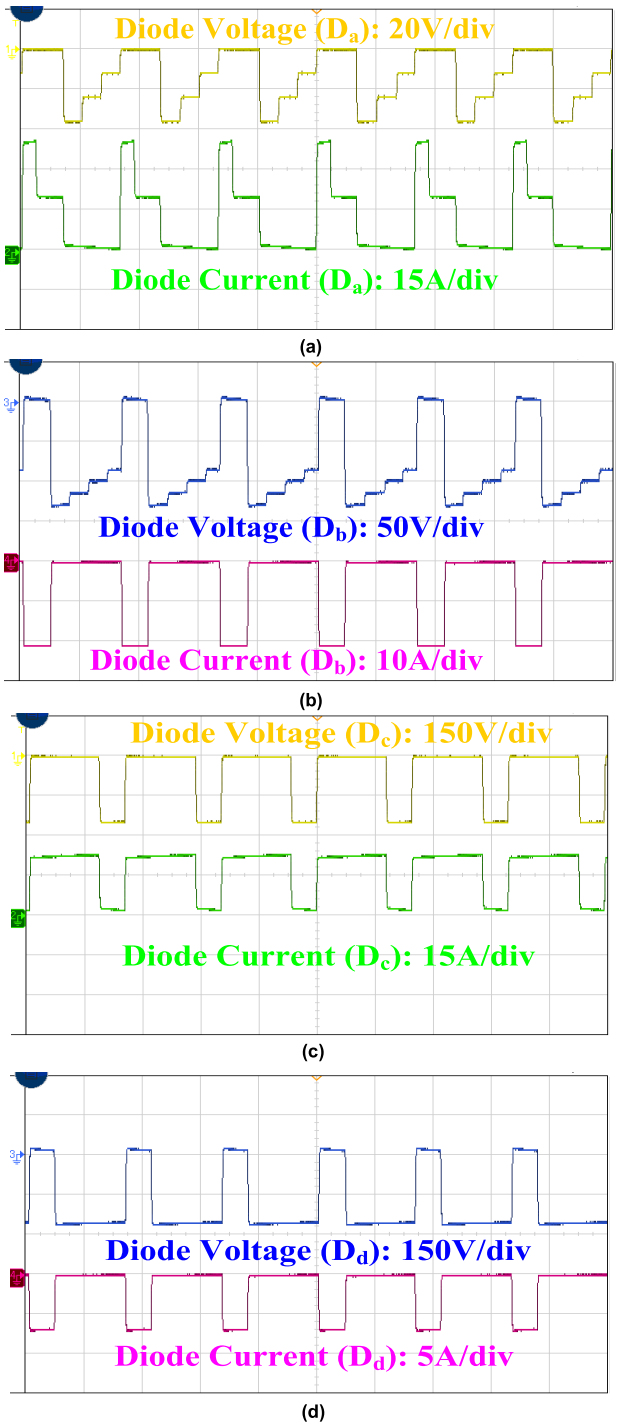

FIGURE 17. Simulation waveforms of step variation in input supply voltage.

and C_{01}. Using these values, we can derive the transfer functions of the output voltage concerning the control variables, as shown in the equations. Additionally, we can use an adjunct polynomial scheme to simplify the higher-order transfer functions to second-order transfer functions, as demonstrated in the equation (36).

The transfer function for the proposed converter can be written as:

$$\frac{V_O}{\hat{d}_1} = \frac{-D_1 D_2 D_3}{(1-D_1)(1-D_2)(1-D_3)(s^2 L_a L_b C_1 C_{01})} + \frac{D_1 D_2}{(1-D_1)(1-D_2) R_{01} C_1 s} + \frac{D_1 D_3}{(1-D_1)(1-D_3) R_{01} C_{01} s} + \frac{D_2 D_3}{(1-D_2)(1-D_3) L_b C_{01} s^2} \quad (35)$$

where,

The switches Sa, S_b, and S_c have duty ratios of D_1,D_2, and D_3 is 20%. L_a and L_b are the inductances of the two inductors with 5mH. C_1 and C_{01} are two capacitances with 100μF. R_{01} is the load resistance of 300Ω, and s is the complex frequency

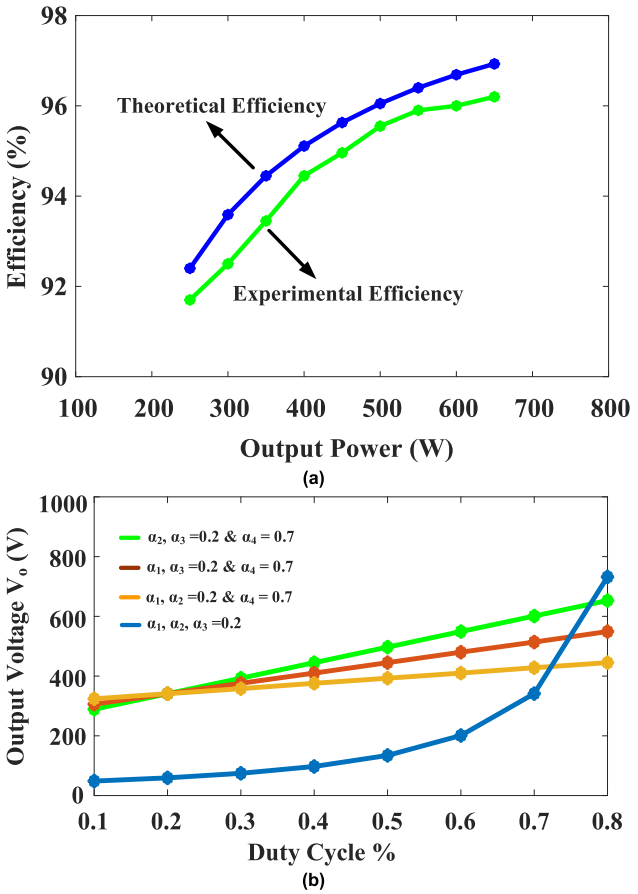

FIGURE 18. (a) Experimental and theoretical waveform of output power and efficiency (b) Output voltage for various duty ratio for proposed converter.

variable. Substituting the given values and simplifying the expression, we get:

$$\frac{V_O}{\hat{d}_1} = \frac{-0.008\ s\text{^}2 + 0.2\ s}{(s\text{^}2 + 1000\ s + 0.0001)} \tag{36}$$

The step response for the proposed converter in an open loop system is shown in Fig. 13. Based on the step response of the transfer function; it appears that the system is currently unstable. However, it may be possible to stabilize the proposed converter by designing a conventional controller.

VI. HARDWARE REALIZATION EXPERIMENTATION RESULTS AND DISCUSSION

The prototype of the proposed FPC is implemented in the laboratory to validate the theoretical analysis and performance of the converter, as shown in Fig. 14. The appropriate minimum and maximum duty ratios have been selected at 0.2 and 0.7 for safe operation in the proposed converter. The pulse for switches S_a, S_b, S_c, and S_d are generated with a switching frequency of 20kHz using Opal RT HIL FPGA (OP4512) real-time simulator. The Itech power supply with solar array simulation software (SAS1000) is used as the PV source. Lithium Ion battery and Rigol power supply is used as another sources. The analysis of experimental results is precisely harmonized with obtained analysis of simulation and noticed from presented waveforms.

TABLE 6. Summary of presented topology.

Topology	Advantages	Disadvantages
[18]	• Voltage stress is low; • High output voltage level; • Continuous input current.	• Number of components will increase depends on design;
[24]	• High voltage gain; • Device count is less.	• Unable to provide high conversion ratio; • Doesn't have continuous current.
[26]	• voltage and current stress are low; • Capability of using active-passive cell; • Conversion gain.	• High number of semiconductor devices; • High cost
[30]	• Snubber circuit is easier to design, reliable, and cost-effective; • Improvement of the switching frequency of the converter; • conversion gain can be flexible.	• High number of elements; • Low power applications.
[32]	• Capability of utilizing different type of voltage sources with different V-I characteristics; • Continuous input current; • No need to any transformer; • Modular Capability.	• Unidirectional power flow.
[33]	• Need to only one inductor • Capability of combining buck and buck-boost converters; • Common output filter.	• High value of input current ripple; • Lack of capability to act as a multilevel dc/dc converter.
[34]	• Bidirectional power flow; • Capability of buck, boost, and buck-boost operation; • Capability of generating positive voltage without using any transformer.	• High cost • Supplying load by only one of the sources.

The electrical specification for experimental parameters is given in Table 5.

Fig.15 shows the voltage and current waveforms of output and inductors. As shown in Fig.15 (a), the maximum output voltage is about 310V, and the average output current is 2A. The experimental waveform of voltage and current across two inductors L_a and L_b are shown in Fig. 15 (b – c). The inductors L_a is observed to be energized during the first four modes of operation with 48V, 36V, 24V, 12V, and deenergized with – 75V, respectively. The inductor L_b is observed to be energized with 115V, 103V, 91V, 79V in first four modes and de-energized with –230V in last mode of operation, respectively. The average current value through the inductors L_a and L_b are 25.4A and 7.8A, correspondingly. The current and voltage waveform across switches S_a, S_b, S_c and S_d is outlined in Fig. 16. The maximum voltage across the switch S_a, S_b, S_c, S_d is clearly perceived to 36V, 24V, 12V, 310V, respectively, is shown in Fig.16(a – d). The average current through all the switches is 30A.

The current and voltage waveforms of diodes D_a, D_b, D_c, D_d is outlined in Fig. 17. The peak voltage across the diodes D_a, D_b, D_c, D_d are 36V, 120V, 230V, and 305V is outlined in Fig.17 (a – d). The average current through all the diodes is 19A, respectively. From the experimental results, it is evident that the proposed converter is able to provide high voltage gain, and efficiency with voltage stress on switches is reduced.

Fig.18 (a) shows the experimental and theoretical values of output power with respect to efficiency. The experimental efficiency of the proposed converter is 95% for different load conditions, and also average deviation between theoretical and experimental efficiency is around 1%. Fig.18 (b) shows that the proposed converter provides voltage gain by appropriately varying the duty ratios to the switches. The advantages and disadvantages of paper contributions has been described in table 6.

VII. CONCLUSION

A New FPC converter is proposed with three input sources with high voltage gain, voltage stress across the switch is low, and the input and output grounding is common are merits of the proposed converter. The converter structure can be modified to function as a multiple-input high-gain dc-dc converter, allowing it to interface any number of input sources. In-depth illustrations were provided of the equivalent circuits and modes of operation for the high gain boost operation. The output voltage equations for all of the aforementioned FPC operations were derived. Simulation results were presented to demonstrate the viability and effectiveness of the suggested converter. The experimental findings demonstrate the FPC's satisfactory performance. The converter structure for n-input and m-output, the impact of parasitic components on the output voltage and efficiency, performance comparisons with recently reported similar topologies, etc. are some of the future focuses of this work.

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