IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 2 October 2023, accepted 18 October 2023, date of publication 23 October 2023, date of current version 27 October 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3326752

RESEARCH ARTICLE

Novel Isolated Multiport DC Converter With Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids

IMMANUEL NINMA JIYA[1], (Student Member, IEEE), HUYNH VAN KHANG[1], PASAN GUNAWARDENA[2], (Student Member, IEEE), NAND KISHOR[3], (Senior Member, IEEE), AND YUNWEI RYAN LI[2], (Fellow, IEEE)

[1]Department of Engineering Sciences, University of Agder, 4879 Grimstad, Norway
[2]Department of Electrical and Computer Engineering, University of Alberta, Edmonton, T6G 1H9, Canada
[3]Faculty of Engineering, Østfold University College, 1671 Halden, Norway

Corresponding author: Immanuel Ninma Jiya (immanueljiya@ieee.org)

This work was supported in part by the Research Council of Norway through the project "Integrated Renewable Resources and Storage: Operation and Management" under Grant 285545; and in part by the University of Agder, Norway, under Grant 63828.

ABSTRACT Due to their greater reliability, efficiency, and resilience as compared to unipolar dc grid systems, bipolar dc grid systems are swiftly gaining popularity for the integration of renewable energy sources. However, development of multiport converters for bipolar microgrid systems is still progressing slowly in terms of reducing costs or improving power density and compact designs. This paper proposes a multiport isolated dc-dc converter with naturally symmetric bipolar outputs (MIBDC). With respect to the number of input ports, voltage gain, and output symmetry that the proposed converter naturally possesses, it outperforms its few competitors. Additionally, the proposed MIBDC significantly reduces component count and control complexity by employing a fixed transformer with only one primary and secondary winding for any number of inputs. The suggested converter's performance in both open and closed loops is evaluated quantitatively in simulation and experimentally using OPAL-OP5700 RT's hardware-in-the-loop (HIL) platform under various situations.

INDEX TERMS Bipolar dc converter, hardware-in-the-loop (HIL), multiport converter.

I. INTRODUCTION

The hunt for green alternatives has gained traction in recent years due to the impending exhaustion of fossil fuels and the damaging environmental effects of using them to meet rising energy demands [1]. It has been demonstrated that fuel cells, wind, and photovoltaic (PV) systems are appropriate alternatives to offer the urgently required green solutions [2]. The rising use of these renewable energy sources (RESs) has caused a paradigm change in the production and use of electrical energy, moving it from centralized to distributed generating systems [3], many of which are often based on dc microgrids. The three-wire dc bus grid technology known as bipolar dc grids (BDCG) is gradually gaining acceptance as a method to enhance dc microgrids. This quick adoption is a result of BDCGs' greater efficiency, as they use less current to transport the same amount of electricity than unipolar dc grids (UDCGs) do. Additionally, BDCGs are more dependable than UDCGs because even if one of the poles fails, the remaining pole may still transfer electricity, although at a reduced capacity. Further, converting from dc to ac voltage with multilevel inverters (MLIs) is simpler and more reliable with BDCGs than with UDCGs. This is because BDCGs have three voltage levels ($\pm\frac{V_o}{2}$ and V_o) and UDCGs have only one level. Due to these desirable characteristics of BDCGs, RESs and dc loads may now be more effortlessly integrated utilizing dc-dc converters [4]. However, because the voltage of the multiple sources and loads differs significantly,

The associate editor coordinating the review of this manuscript and approving it for publication was Jahangir Hossain.

many single-input single-output (SISO) dc-dc converters are needed to step-up or step-down the voltage to or from the BDCG system. Due to global shortages of semiconductor chips, several components, particularly semiconductors, are therefore needed in addition to bulky and complicated setups and high costs [5].

Consequently, a solution to the aforementioned issues with SISO dc-dc converters has been proposed: multiport dc-dc converters (MPCs), which are often developed from traditional SISO converters [6], [7], [8], [9]. There are numerous MPCs with and without galvanic isolation that have been proposed as a result of extensive research into MPCs. Isolated MPCs provide substantial advantages over non-isolated MPCs in terms of soft switching capability, high gain, and safety thanks to the magnetic isolation of input and output provided by the magnetic components. In [6] and [7], MPCs with multiple-inputs and single-outputs (MISO) based on half-bridge, full-bridge (FB), dual active bridge (DAB) and multi active bridge (MAB) converters, have been proposed. However, a common limitation of these converters is the use of multiple windings for the inputs of transformers or coupled inductors based on flux additivity. As a result, the size and control complexity rise and the power density decreases. Numerous clamping circuits may be necessary due to the need for multiple windings on the primary side of the magnetics for each input source, which would increase component count and perhaps control complexity if an active clamping is being used. The authors in [8] and [9] suggest isolated MPCs with just two windings, a primary winding and a secondary winding, to allay these issues. Given that they all have a single output port, they are all inadequate for BDCG systems. In order to address this, MPCs with multiple inputs and outputs (MIMO) have been proposed in [10] and [11]. However, these MIMO MPCs are afflicted by cross-regulation of the voltage at the output ports, necessitating the use of sophisticated controllers. Due to this issue, bipolar dc-dc converters (BDCs) were developed. These converters normally only have two symmetrical outputs, one for each pole (positive and negative, respectively). To that end, BDCs have been proposed in [12], [13], [14], [15], and [16], but as they are all single input converters, they share the same problems as SISO converters, which have been described previously. Multiport bipolar dc converters (MBDCs) have recently been suggested in [17], [18], [19], and [20] as a solution to this problem. The non-isolated MBDCs in [17] and [18] have low gain, poor power density, and only two inputs to the MPC; as a result, they cannot be expanded to include an arbitrary number of inputs, which is one of the main characteristics of MPCs. Due to the lack of magnetic separation, they also pose a safety risk. Even though the multiport isolated bipolar dc converters (MIBDCs) in [19] and [20] are the only MIBDCs that have been suggested in the literature thus far, in certain circumstances, their feature soft switching in some cases is just like their non-isolated counterparts in [17] and [18]. Despite the need for sophisticated control to maintain balanced symmetric output voltages, none of them can support arbitrary independent power flow from either of the input sources to the bipolar dc bus. Further, they both have a finite number of inputs and low voltage gains. To address these drawbacks, novel MIBDCs are necessary. Moreover, there have been less isolated MPCs with bipolar naturally symmetric outputs proposed in literature than there have been for their unipolar equivalents. Further, the implementation of maximum power point tracking (MPPT) in MPCs for the integration of multiple RESs continues to pose a challenge. This is evidenced in [21], [22], and [23], in which MPPT is implemented for only one input source or in a rather complex way, where one controller is required for each input.

The MIBDC developed in this article solves the limitations of prior topologies by adopting a DAB-based and FB-based topology with a fixed two winding (one primary and secondary winding each) transformer and several ports built utilizing pulsing voltage sources. A single inductor is time multiplexed to provide any arbitrary independent and concurrent power transmission from numerous sources while the component count is maintained to a minimum. The proposed MIBDC is unique in the following ways:

1) Regardless of the number of input sources, only one primary and secondary winding is required.
2) It can transmit power from the inputs to the dc bus independently and concurrently.
3) With bipolar output voltages and high gain, it can perform unidirectional buck and boost operations.
4) When additional input is introduced, a reverse blocking switch can be added to raise the number of inputs at will.
5) The symmetrical nature of the bipolar output voltages is intrinsic.
6) The converter simply needs a single input single output (SISO) controller, such as the common double loop PI controller, and has a very simple control framework.
7) In addition, a distributed MPPT (DMPPT) approach is suggested to lessen complexity and make it possible to use a single MPP controller for any number of inputs.

Within this framework, the new MBDC was analyzed for two input sources with equal and different input voltage levels, put through extensive simulations, and experimentally verified. The initial idea of the MIBDC proposed in this work has been presented in [24]. In this paper, the detailed analysis and features are numerically verified and results from experimental validation using the HIL test rig is presented. HIL verification has been proved to accurately and sufficiently prove the operation of power converters [25] and as such is implemented in the verification of the proposed MIBDC.

II. PROPOSED MIBDC TOPOLOGY

The proposed multiport isolated dc-dc converters with bipolar symmetric outputs are shown in Figure 1. These MIBDCs are constructed by combining a conventional DAB or a phase-shifted full bridge (PS-FB) converter with a secondary side center tapped transformer to produce outputs with bipolar symmetry. To regulate the output voltage and make it

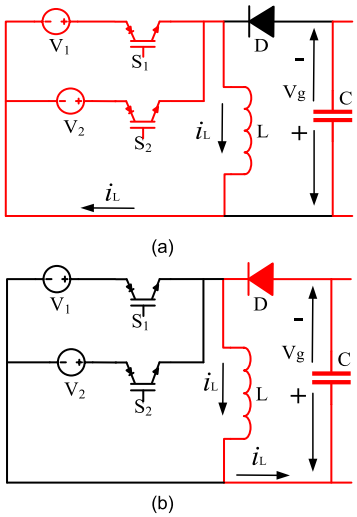

FIGURE 1. Path of current flow in in the multiport section during (a) charging and (b) discharging of L, for simultaneous power flow with two inputs.

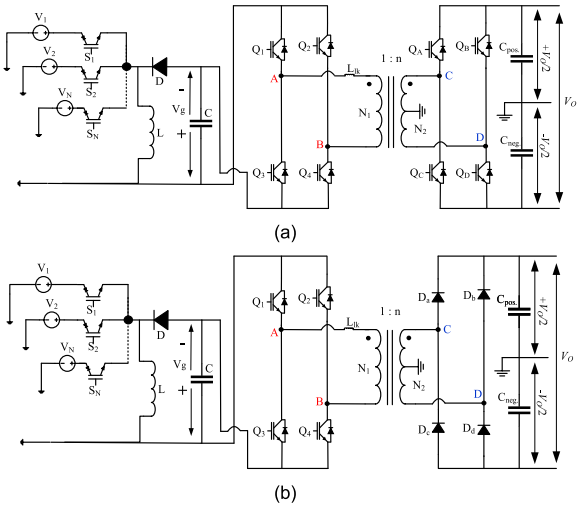

FIGURE 2. Proposed (a) dual-active-bridge and (b) full-bridge -based bipolar multiport dc-dc converter.

easier to include inputs of different voltage levels, the numerous inputs are achieved using pulsing voltage sources and a time multiplexed inductor charging technique. The converter in Figure 1 (b) is proposed as a way to simplify the control of the DAB section in Figure 1 (a) by swapping out the secondary active bridge in Figure 1 (a) with a diode H-bridge in Figure 1 (b). As a result, it is similar to a standard PS-FB converter with the addition of secondary side center tapping of the isolation transformer to enable bipolar outputs. Both topologies in Figure 1 have the same multi-input power processing mechanism, involving reverse blocking switches S_1 to S_N, one diode, capacitor, and inductor, respectively. Reverse blocking switches are used to make it easier to integrate several sources with different voltage levels while maintaining independent and simultaneous power flow from the sources. It is noteworthy that the market options for reverse blocking switches are few although it is receiving attention in research [26]. Another alternative method to realize an RBS is to place a diode in series with the switch to block reverse flow of current. Additionally, the converters may supply $\pm V_o/2$ and V_o on the dc lines at three different voltage levels. Since the key operating principles described are essentially transferable from the PS-FB to the DAB based MIBDC, the MIBDC proposed in Figure 1 (b) will be analyzed for two inputs under independent and simultaneous energy transfer configurations for the steady state continuous conduction mode (CCM) analysis in this paper.

A. INDEPENDENT POWER FLOW

In the case of two-inputs to the proposed MIBDC, power can flow from either of the inputs (V_1 or V_2) to the bipolar dc bus in the independent power flow mode of the proposed MIBDC. In order to charge the inductor, L, for a duration of DT_S, where D is the duty cycle and T_S is the total switching period, the corresponding switch controlling each input source, S_1 for V_1 or S_2 for V_2, is switched ON. Diode, D, conducts in the direction shown in Figure 2 (b) to discharge L during (1-D)T_S, the switch's OFF period. Resultantly, the multiport portion functions like a typical inverting buck-boost converter, and capacitor C has a voltage that matches the description in (1). The PS-FB part and the multiport section both function simultaneously when the multiport section is active, as shown in Figure 3. The MIBDC's isolation transformer section is run in a fashion that causes zero voltage switching on the active switches Q_1 through Q_4 (ZVS). A thorough explanation of the ZVS function is presented in [27]. The steady state waveform in Figure 3 displays the pulse signal for these switches. To account for the phase shift ($\emptyset$) and the deadtime necessary to accomplish ZVS, the total switching period for Q_1 through Q_4 is divided into 10, (t_0 to t_{10}). The connection between the input voltage and the dc link is represented by (2), where n is the turn ratio (N_S/N_P) of the transformer, during steady state CCM operation.

$$V_g = \frac{V_{in}D}{1-D} \tag{1}$$

$$V_o = \left(\frac{V_{in}D}{1-D}\right) 2\phi n = 2V_g\phi n \tag{2}$$

B. SIMULTANEOUS POWER FLOW

The converter shifts to simultaneous power flow mode when energy from more than one input must be transferred to the dc link, as shown in Figure 2 for two inputs. The switches S_1 to S_N that control all the sources are turned ON simultaneously but are thereafter switched OFF in the sequence of the various voltages' descending magnitudes. As a result, the charging of L is time multiplexed, as described in [28] and [29] and shown in Figure 3, permitting the simultaneous transfer of power from two inputs.

According to Figure 3, the charging and discharging durations of L make up the two main segments of the switching

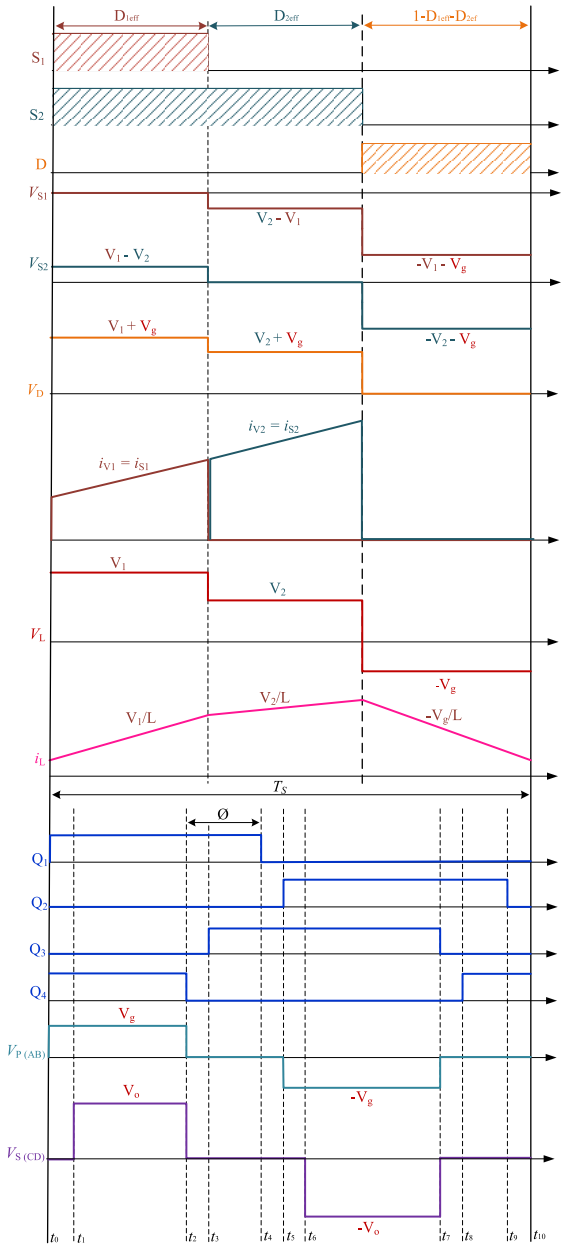

FIGURE 3. Steady state key waveforms of the phase-shifted full-bridge based multiport bipolar dc-dc converter.

period in steady state CCM. The second component stays set as $(1 - \sum_{i=1}^{N} D_{ieff})$, showing the discharging time of L. The first part is further split based on the number of inputs of the MIBDC operating simultaneously: two divisions (D_{1eff} and D_{2eff}) in this case, since the MIBDC is being analyzed for two inputs. The current flows from the source with the highest potential first when the switches are turned ON, which is V_1 in this case. As a result, L is charged with a slope of V_1/L during D_{1eff}. After D_{1eff}, V_2 assumes control and starts charging L with a slope of V_2/L during D_{2eff}. With a slope of V_N/L for any number of inputs, this goes on until D_{Neff}. At the conclusion of the charging period, L is discharged with a slope of $-V_g/L$. Additionally, the PS-FB part is functioning concurrently with the multiport section, as shown in Figure 3. Through implementing volt-second equilibrium to the resultant steady state CCM waveform in Figure 3, capacitor C's voltage is described by (3) and the input-output voltage is specified by (4).

$$V_g = \left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3}$$

$$V_o = \left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] 2\phi n = 2V_g \phi n \tag{4}$$

To accomplish simultaneous power transmission to the load, certain criteria must be adhered to for the switches to commutate effectively in multi-input mode. When the voltages are not identical, the sources' magnitudes are randomly placed in decreasing order so that $V_1 > V_2 > \ldots > V_N$. Further, it is required that the duty cycles of the PWM signals used to regulate the input source switches, e.g. S_1 and S_2, be such that $D_1 < D_2 < \ldots < D_N$, and vice versa, where $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, $\ldots$, $D_N = D_{1eff} + D_{2eff} + \ldots + D_{Neff}$. To obtain equal power supply from the sources, the duty cycles of the PWM signals must be set so that $D_1 = D_2 = \ldots = D_N$ if the source voltages are equal, such that $V_1 = V_2 = \ldots = V_N$. In the event that the sources' necessary power delivery is not equal, the magnitudes of $D_1, D_2, \ldots, D_N$ can be computed in the sequence of the required power delivery from each source.

C. TRANSFORMER AND SOFT SWITCHING

The MIBDC incorporates an isolation transformer section where the active switches, $Q_1 - Q_4$, are carefully controlled to ensure zero voltage switching (ZVS) during their operation. A comprehensive description of this operational mechanism can be found in [27], with a condensed summary provided in this section. The pulse signal corresponding to these switches is displayed in the steady-state waveform illustrated in Figure 3. To achieve ZVS, the total switching period of $Q_1 - Q_4$ is divided into ten intervals, denoted as $t_0 - t_{10}$. This division allows for accommodating the necessary phase shift ($\emptyset$) and deadtime required for ZVS. At the beginning of the cycle, specifically at t_0, both Q_1 and Q_4 are turned on, with Q_1 already in the on-state and Q_4 turned on at t_8 during the previous cycle. These switches are activated in a manner that ensures ZVS. The voltage across the secondary winding (V_S) remains at zero until t_1, when the current in the primary winding reverses to a positive direction. Consequently, V_S becomes equal to $2nV_g$ or V_o, and the voltage across the primary winding (V_P) is equal to V_g. During the operation of the system, diodes D_a and D_d are biased in the forward direction to charge capacitors $C_{pos.}$ and $C_{neg.}$, respectively. The charging process occurs up to $\pm V_o/2$, with $C_{pos.}$ being charged for the positive pole and $C_{neg.}$ for the negative pole. This results in a voltage of V_o across the entire

DC link, which also supplies the load. At time t_2, the active switch Q_4 is deactivated, resulting in V_P and V_S reaching zero. After a specified deadtime ($t_3 - t_2$), the switch Q_3 is activated with ZVS achieved at time t_3. Similarly, at time t_4, Q_1 is deactivated, and after the deadtime ($t_5 - t_4$), Q2 is activated with ZVS. This causes V_P to transition to $-V_g$, and the primary current starts reversing its direction, gradually becoming entirely negative by time t_6. Consequently, V_S also shifts to $-V_o$. During the time interval between t_3 and t_6, the diodes $D_a - D_d$ are biased in the reverse direction, causing the discharge of capacitors $C_{neg.}$ and $C_{pos.}$. These discharged capacitors provide the necessary power supply to the loads until time t_6 when the diodes D_2 and D_3 are forward biased. At time t_7, the switch Q_3 is turned off, followed by the activation of switch Q_4 after the specified deadtime ($t_8 - t_7$) at time t_8, achieving ZVS. At time t_9, the switch Q_2 is turned off, and after a specified deadtime ($t_{10} - t_9$), the cycle returns to t_0 when the switch Q_1 is turned on again with ZVS. This makes t_0 and t_{10} essentially identical. During the time interval between t_6 and t_8, the capacitors $C_{neg.}$ and $C_{pos.}$ are charged, and then they discharge power to the load between t_8 and t_1 when the diodes $D_a - D_d$ are biased in the reverse direction.

From the basic transformer-turns ratio equation (5), the natural voltage symmetry of the proposed converter is achieved through the center tapped transformer. Since the transformer is center tapped, the turns ratio-voltage equation is presented in (6). Therefore, as long as the transformer tapping remains central, the natural voltage symmetry of both poles is maintained. Other parameters such as the stress and selection of the components are as presented in [29] and [30].

$$\frac{V_{AB}}{V_{CD}} = \frac{N_1}{N_2}; V_O = V_{CD} = \frac{N_2}{N_1} V_{AB} \tag{5}$$

$$\pm\frac{V_O}{2} = \frac{V_{CD}}{2} = \frac{(N_2/2)}{N_1} V_{AB} \tag{6}$$

D. VOLTAGE GAIN

When compared to the single input forms from which they are developed, the voltage gain of multiport converters is somewhat different [31]. Therefore, voltage transformation factor (V_{TR}) is the ideal way to describe multiport converter gai. VTR is expressed as in the case of the proposed converters (7). At an effective duty cycle (D_{ieff}) of 90%, the proposed converter may produce a high gain of up to $20\emptyset n$. Thus, if a bigger gain is necessary, the phase shift ($\emptyset$) and turns ratio (n) can be employed to further improve the converter gain.

$$V_{TR} = \left[V_o \Big/ \left(\sum_{i=1}^{N} V_i D_{ieff} \right) \right] = \left[(2\phi n) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff} \right) \right] \tag{7}$$

E. CONTROL STRUCTURE

Figure 4 shows the control structure of the proposed MIBDC. The control layer consists of the secondary controller (with the DMPPT controller), the double loop PI controller, the power management controller (PMC), phase shift (PS) controller and the respective pulse width modulators (PWM). The secondary controller sets the output voltage reference (V_{g-ref}) of the multiport section, depending on the required operating mode of the MBDC and the MPP of input sources. The MPP controller is also responsible for the proportion of power flow from the sources when operating in a simultaneous power flow mode. To do this, the MPP controller determines scaling factors k_1 to k_{N-1}, which are obtained by implementing an DMPPT algorithm for sources (V_1 to V_{N-1}). Figure 5 shows the flowchart of DMPPT, in which the classic perturb and observe (P&O) algorithm is implemented. The output of the DMPPT P&O algorithm is k_1 to k_{N-1}. V_O and i_L are used to determine the control variable β, which is the time required to charge the inductor(s). The PI gains of the double loop PI controllers are selected heuristically. The PMC based on the scaling instructions (k_1 to k_{N-1}.) from the DMPPT controller determines $D_{1eff} - D_{Neff}$ and the respective duty cycles according to (8). Further, the PS-controller provides

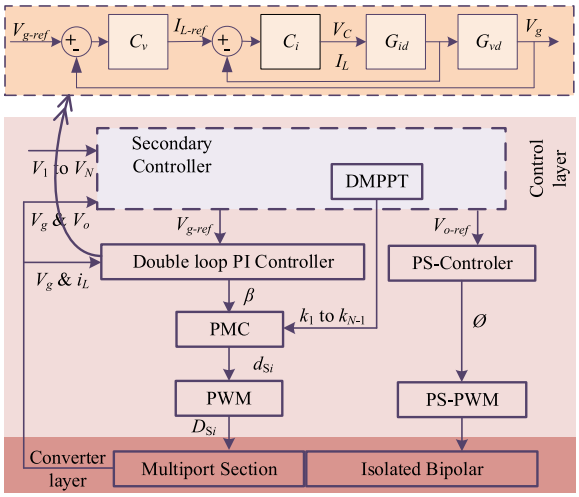

FIGURE 4. Control structure of the proposed MIBDC.

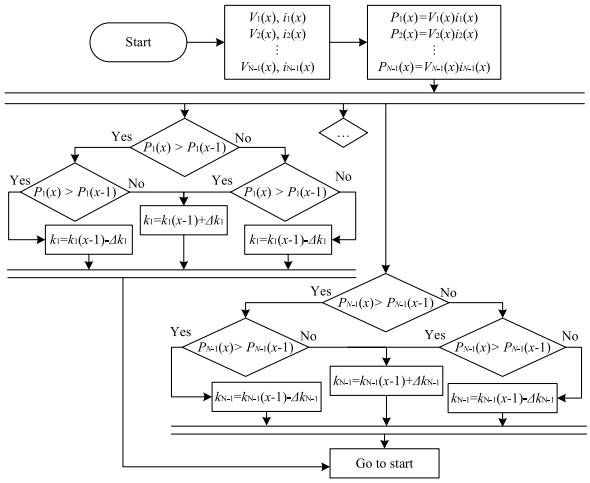

FIGURE 5. Flowchart of DMPPT controller of the proposed MIBDC.

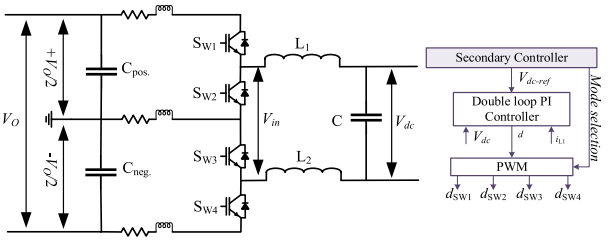

FIGURE 6. Schematic of bipolar to unipolar dc-dc converter for critical loads.

TABLE 1. Switch conduction in the bipolar to unipolar converter for critical loads.

State	V_{in}	T_1	T_2
Healthy state	V_O	S_{W1} S_{W4}	D_{W2} D_{W3}
Failure in positive line	$V_O/2$	S_{W4}	D_{W2} D_{W3}
Failure in negative line	$V_O/2$	S_{W1}	D_{W2} D_{W3}
Failure in neutral line	V_O	S_{W1} S_{W4}	D_{W2} D_{W3}

the required phase shift (Ø) required to keep the output voltage of the isolated bipolar section constant based on the target output voltage (V_{o-ref}).

$$\left.\begin{aligned} D_{1eff} &= k_1\beta \\ &\vdots \\ D_{N-1eff} &= k_{N-1}\beta \\ D_{Neff} &= \beta - \sum_{i=1}^{N-1} D_{ieff} \end{aligned}\right\}, \left\{\begin{aligned} d_1 &= D_{1eff} \\ d_2 &= D_{1eff} + D_{2eff} \\ &\vdots \\ d_{N-1} &= \sum_{i=2}^{N-1} D_{ieff} \\ d_N &= \sum_{i=1}^{N} D_{ieff} \end{aligned}\right\} \quad (8)$$

F. RESILIENT OPERATION FOR CRITICAL LOADS

One key advantage of bipolar dc power systems over the unipolar counterparts is the increased reliability of power supply for critical load units. This is demonstrated by the ability to continue to supply power to the critical load unit in the event of a failure or open circuit fault in any of the lines of the bipolar system. Figure 6 presents the schematic of a bipolar to unipolar dc-dc converter required to achieve this. The bipolar to unipolar dc-dc converter is essentially a cascade of two synchronous buck converters and its operation is similarly so. The switching pattern of the converter is presented in Table 1 for the healthy state and fault states. The input-output voltage relationship of the converter is described by (9), which is basically the same as a traditional buck converter's. The input voltage (V_{in}) in this case depends on the state of the bipolar dc, under healthy state and failure in the neutral line, V_{in} is equivalent to V_o while it is equivalent to $V_o/2$ in the other two fault states.

$$V_{dc} = V_{in}D \quad (9)$$

III. RESULTS

Utilizing the OPAL-RT OP5700 device, which runs a 64-bit Virtex-7 FPGA, the proposed isolated MIBDC is quantitatively verified in simulation and validated experimentally.

TABLE 2. Parameters used in verification.

Parameter	Value	Unit
Inductor (L)	1	mH
Capacitors (C=$C_{pos.}$=$C_{neg.}$)	4.7	µF
Voltage sources (V_1/V_2)	100/75	V
Transformer turns ratio (n)	2	
Phase shift ($Ø$)	27	degrees
Switching frequency (Fsw)	20	kHz

Figure 7 depicts the configuration for the laboratory experimental validation. Table 2 provides the parameter values for each component. In both closed and open loop operations, the topology of the MIBDC was evaluated. Five scenarios involving open loop operation were run, the first two of which represented independent power flows from the two sources (V_1 and V_2) to the dc link, respectively. The MIBDC is operated in both simultaneous power flows from both sources with equal and uneven voltage levels in the remaining three open loop situations. Finally, the converter was run in a closed loop to test the bipolar outputs' capacity to naturally maintain symmetry.

A. VERIFICATION OF SINGLE INPUT OPERATION

The open loop verification of running the MIBDC with the first voltage source, V_1, and the second voltage source, V_2, providing the bipolar dc link separately is shown in Figures 8 and 9, respectively. For both scenarios, V_1 is set to 100 V, V_2 is 75 V and the results presented include inductor current (i_L) and voltage (V_L), primary (V_P) and secondary (V_S) turns voltage of the transformer, input currents, voltages of S_1 (i_{S1}, V_{S1}), S_2 (i_{S2}, V_{S2}), the dc link (i_{dc} and V_{dc}), and the voltage across the switches of the PS-FB section, $V_{Q1} - V_{Q4}$ and $V_{Da} - V_{Dd}$. The result of V_1 alone delivering power to the dc link is shown in Figure 8. To do this, S_1's switch duty cycle, D_1, which controls the first voltage source, V_1, is set to 0.4, while S_2's duty cycle, D_2, is set to 0. There was a 200 Ω load over each pole and the full dc link. The results shown in Figure 8 match numerical solutions with $\pm V_o/2$ and V_o at about ±123 V and 245 V, respectively, and $\pm i_o/2$ and i_o at about ±0.6 A and 1.2 A. In Figure 9, the results of independent power flow from V_2 are presented. D_1, the duty cycle of S_1 was set to 0, while that of S_2, D_2 was set to 0.4. The load across each of the voltage levels was also 200 Ω each. Again, the results in Figure 9 show good agreement with numerical solutions. In Figure 9, the independent power flow results from V_2 are shown. D_1, S_1's duty cycle was set to 0, and S_2's duty cycle was set to 0.4. The load was 200 Ω across each voltage level as well. Once more, the results in Figure 9 exhibit strong congruence with numerical results such that $\pm V_o/2$ and V_o being about ±90 V and 180 V respectively and $\pm i_o/2$ and i_o at about ±0.45 A and 0.9 A respectively.

B. VERIFICATION OF SIMULTANEOUS OPERATION

The outcomes of the final three open loop operating scenarios—i.e., the simultaneous transmission of power from

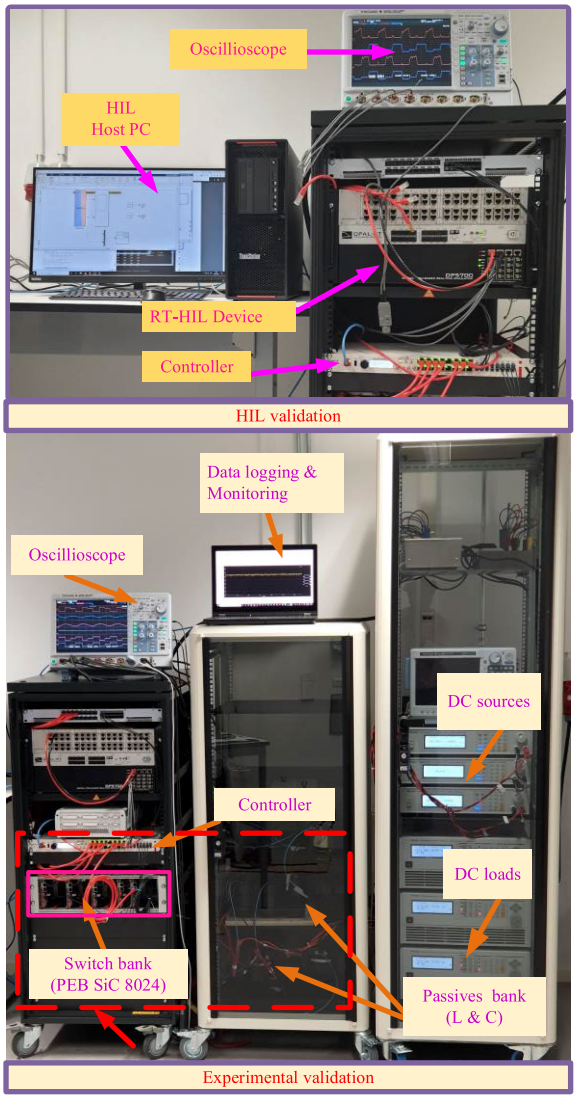

FIGURE 7. In-house HIL platform used for validating the MIC.

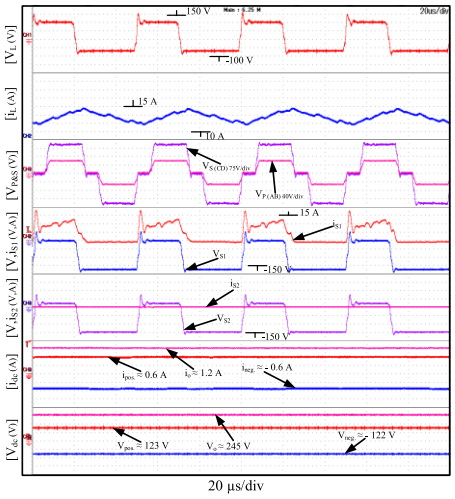

FIGURE 8. Results when only V_1 is supplying the dc bus where V_1 = 100 V, V_2 = 75 V, D_1 = 0.4 and D_2 = 0.

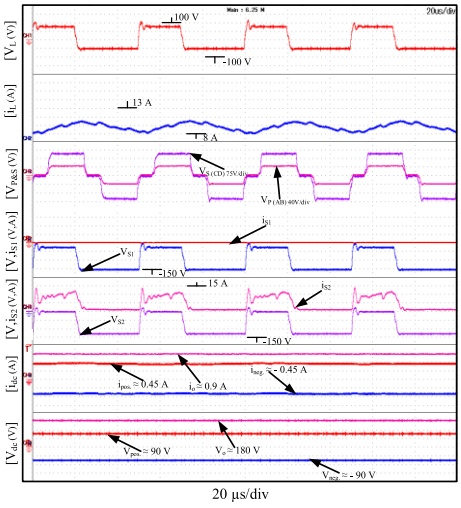

FIGURE 9. Results when only V_2 is supplying the dc bus where V_1 = 100 V, V_2 = 75 V, D_1 = 0 and D_2 = 0.4.

the two inputs to the bipolar dc link—are shown in Figs. 10 through 12. Since Figs. 10 and 11 have the same effective duty, $\sum_{i=1}^{N} D_{ieff}$, of 0.6 and equal input voltages with $V_1 = V_2 = 75$ V, their output characteristics are the same. Therefore, both results in Figs. 10 and 11 are in agreement with the numerical solutions with $\pm i_o/2$ and i_o being about ± 1.0 A and 2.0 A respectively and $\pm V_o/2$ and V_o at about ± 210 V and 420 V, respectively. The main difference with both scenarios is that D_1 was set to 0.3 and D_2 to 0.6 in Figure 10 such that $D_{1eff} = 0.3$ and $D_{2eff} = 0.6$, so since both voltages are equal, while S_1 is ON, S_2 is also ON and both sources are charging the inductor, L, and then when D_1 goes OFF, only D_2 is charging L. Thus, the average i_{S2} is larger than from i_{S1}, while in Figure 11, $D_1 = D_2 = 0.6$ and so since they have equal voltages, both sources are charging the inductor with currents $i_{S1} = i_{S2}$ during the inductor charging. This demonstrates how the duty cycle is employed to regulate the amount of energy supplied by the various sources. When the voltages are changed in the fifth scenario of Figure 12 so that $V_1 = 100$ V and $V_2 = 75$ V, it is necessary to time multiplex the inductor charging. This is as mentioned previously in section II-B in order to send power from both sources to the load simultaneously. In this case, D_1 was set to 0.3 and D_2 to 0.6 such that $D_{1eff} = D_{2eff} = 0.3$. Typically, Figure 12's performance is in line with numerical solutions with $\pm V_o/2$ and V_o being ± 245 V and 490 V, respectively, and the dc link currents at $\pm i_o/2$ and i_o being ± 1.2 A and 2.4 A, respectively.

C. CLOSED LOOP VERIFICATIONS OF THE MIBDC

Additionally, to operate the MIBDC as previously explained and produce a constant output voltage of $\pm V_o/2$ and V_o of ± 100 V and 200 V respectively and later stepped to ± 125 V and 250 V respectively. In Figure 13, some of the closed loop dynamics are shown. To more thoroughly analyze the

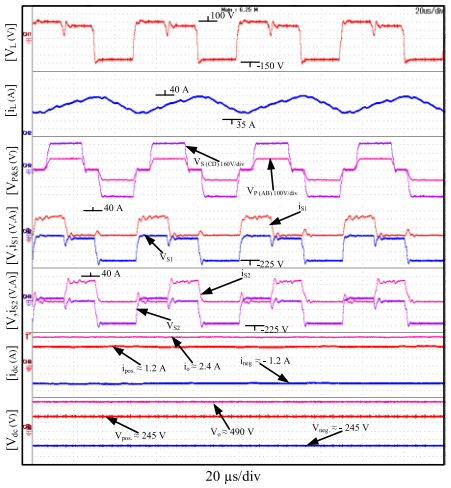

FIGURE 10. Results when both sources are supplying the dc bus where $V_1 = 100$ V, $V_2 = 75$ V, $D_1 = 0.3$ and $D_2 = 0.6$.

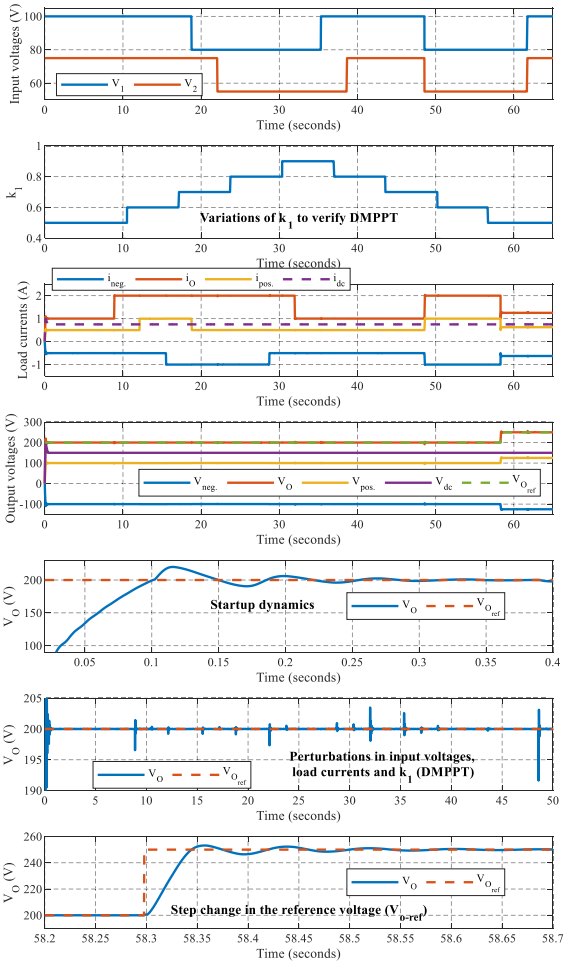

FIGURE 11. Closed loop performance of the MIBDC under perturbations in the input voltages, load currents and output reference voltage.

MIBDC's inherent symmetry properties, the load on the three voltage levels was arbitrarily adjusted. The control target was V_o while the positive and negative poles were left uncontrolled to freely balance the voltage across themself. The load

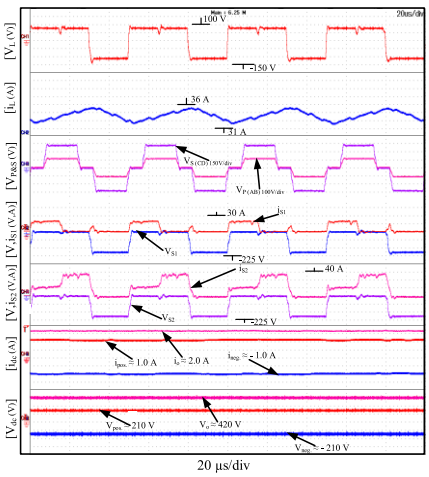

FIGURE 12. Results when both sources are supplying the dc bus where $V_1 = V_2 = 75$ V, $D_1 = 0.3$ and $D_2 = 0.6$.

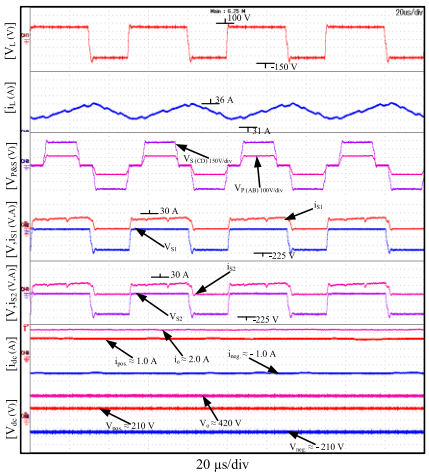

FIGURE 13. Results when both sources are supplying the dc bus where $V_1 = V_2 = 75$ V and $D_1 = D_y2 = 0.6$.

on V_o was doubled from about 1 A to 2 A at 8s and V_o experiences a dip of less than 3 V after that the controller can bring it back to the target 200 V. And then the load on the positive pole was also doubled from 0.5 A to 1 A at 12s and the negative pole's load also doubled from 0.5 A to 1 A at 16s. A voltage sag of less than 1 V was seen on V_o during the load transition for both the positive and negative poles of the MIBDC, but generally, the load changes do not result in an imbalance in the output voltages, which is evidence of the converter's inherent symmetry. A further testament of the MIBDCs' controller is demonstrated in the startup dynamics, where minimal overshoot is observed with a rise time, time constant and settling time of 75ms, 25ms, and 0.25s respectively. Also, a fast response to step change of 50ms is also observed at 58s. Furthermore, the value of k_1 is varied to demonstrate the ability of the MIBDC to use the MPPT to control the power delivered from the input sources without affecting the output voltages. Furthermore, all these

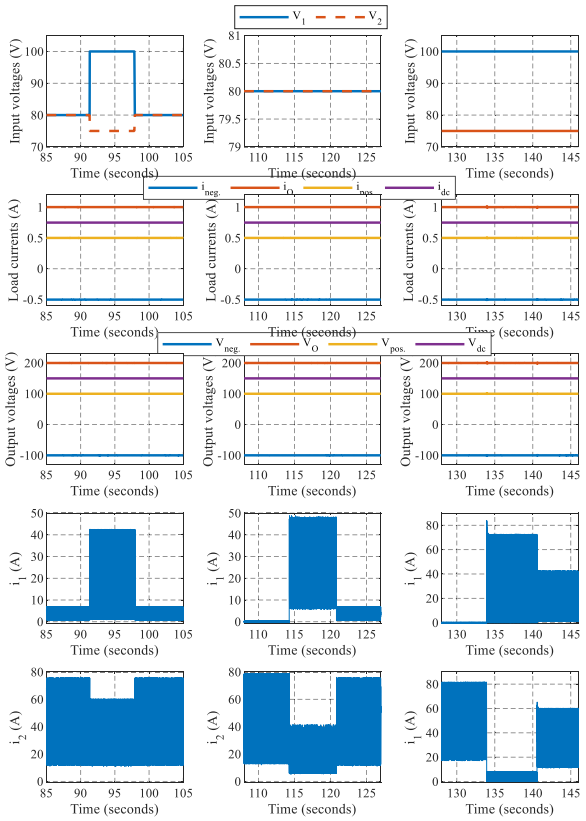

FIGURE 14. Verification of operating mode transitions.

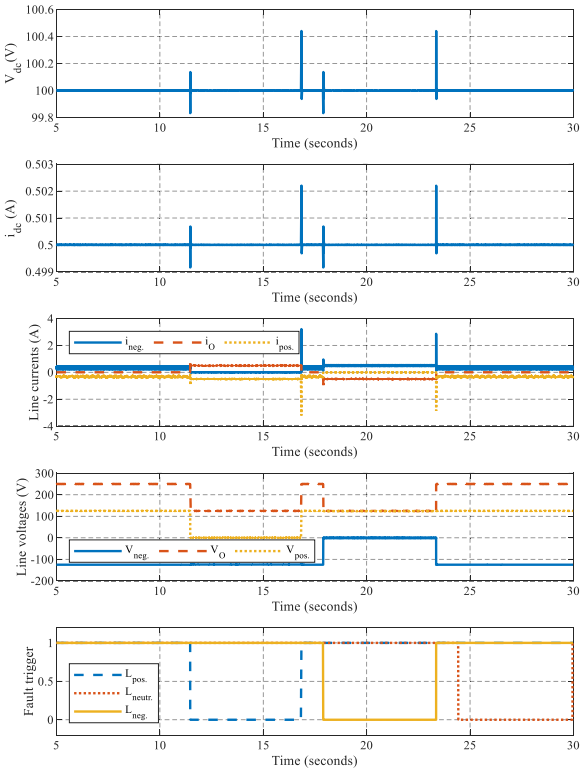

FIGURE 15. Closed loop performance under line failures.

perturbations do not impact the voltage (V_{dc}) or current (i_{dc}) of the critical load. Further, the converter operation under different mode transition is verified with results in Figure 14. The first column presents transitions in the input voltages (V_1 and V_2) from equal (80 V) to unequal (100 V & 75 V) and back to equal (80 V) voltages. The second and third column represent transitions from V_2 alone supplying the dc link to simultaneous power flow to V_1 alone supplying the dc link under equal and unequal voltages respectively in the second and third column. Under all these mode transitions the controller can maintain the output voltages at the target of 200 V and ±100 V. Lastly, in Figure 15, the operation of the bipolar to unipolar converter is verified. Open circuit faults [32] are introduced sequentially in the positive, negative, and neutral lines respectively. Under these faults, the converter can continue to deliver power to the critical load with no significant impact on the quality of the voltage (V_{dc}) or current (i_{dc}) of the critical load.

D. LOSS ANALYSIS

The power losses (P_L) in MIBDC can be estimated using (10), consisting of the inductor and transformer winding (P_W) and core (P_C) losses [33], capacitor losses (P_{Cap}), MOSFET switching (P_{swMOS}) and conduction (P_{onMOS}) losses [34], and the losses in the diode (P_D). Where T_S is the switching period, R_{ESRL} is the inductor's equivalent series resistance (ESR), $\hat{i}_L$ is the inductor average current, Δi_L is the inductor ripple current, K, β&α are Steinmetz parameters, R_{ESRC} is the capacitor ESR, V_{DS} is the MOSFET drain to source voltage, i_{DS} is the MOSFET drain to source current, t_{on}&t_{off} is the MOSFET ON and OFF time, R_{DSon} is the MOSFET on state resistance, D is its respective duty cycle, V_F and i_F are the diodes' forward voltage and current respectively.

$$P_L \approx \left\{ \begin{array}{l} \underbrace{\frac{1}{T_S}\int_0^{T_S} R_{ESR}\left(\hat{i}_L^{\,2} + \frac{\Delta i_L^2}{12}\right)}_{P_W} + \underbrace{K\,\Delta i_L^{\beta} F_{SW}^{\alpha}}_{P_C} \\ + \underbrace{R_{ESRC}\left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}_{P_{Cap}} + \underbrace{\frac{1}{2} V_{DS} i_{DS} F_{SW}\left(t_{on} + t_{off}\right)}_{P_{swMOS}} \\ + \underbrace{R_{DSon} i_{DS}^2 D}_{P_{onMOS}} + \underbrace{\frac{1}{T_S}\int_0^{T_S} V_F i_F^2}_{P_D} \end{array} \right\} \tag{10}$$

Based on (10), the loss distribution in the proposed MIBDC is calculated and presented in Figure 16. P_W accounts for 16%, P_C is 25%, P_{swMOS} is 25%, P_{onMOS} is 16%, P_D is 15% and P_{Cap} is about 3%. The switches and magnetics account for more than 95% of the losses. Therefore, carefully

TABLE 3. Comparison of the proposed family of MIBDCs with existing MIBDCs.

Parameters		Part Count S	D	L	C	Tx	T	No. of inputs	IPF	SPF	Modulable?	Output voltage-symmetry	Soft switching
[20]		6	2	3	2	1	14	2	No	Yes	No	Asymmetrical	ZCS+ZVS
[19]		6	4	2	2	1*	15	2	No	Yes	No	Symmetrical	ZCS+ZVS
Proposed	DAB	N+8	0	1	3	1*	N+13	N	Yes	Yes	Yes	Symmetrical	ZCS+ZVS
	FB	N+4	4										

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, SPF=Simultaneous PF, S=Active switch, D=Diode, L=Inductor, C=Capacitor, Tx=Transformer, T= Total, *=IPF is only possible from the second input port, $^{+}$=PFP is only possible from the first to the second input port and not vice versa, Sw.= Switching.

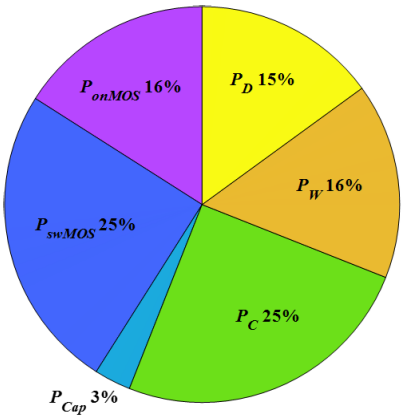

FIGURE 16. Loss distribution in the proposed MIBDC.

selecting and designing the switches and magnetics are vital to maintaining a high efficiency in the proposed MIBDC.

IV. COMPARISON WITH RELATED BIPOLAR MULTIPORT CONVERTERS

Table 3 presents the comparison of the proposed MIBDC with the recently proposed MIBDCs in [19] and [20]. The basis for selecting these MIBDCs for comparison is that, to our knowledge, they are the only existing MIBDCs in literature. Table 3 is arranged in the order of increasing part count, when considering two inputs to the MIBDCs. The proposed MIBDC in [19] has the lowest part count by just 1 but its' output voltage is not inherently symmetrical. And so, a further controller is required to maintain the voltage symmetry on the bipolar outputs. For two inputs, the MIBDCs proposed in this paper has the same part count and symmetrical characteristics as the MIBDC in [20]. But has a key advantage of modularity such that the number of input ports can be arbitrarily increased just by introducing one additional reverse blocking switch. Further, the MIBDCs proposed in [19] and [20] both have a limitation on number of inputs and low voltage gain, areas in which the MIBDCs in this paper are triumphant. Finally, the independent power flow (IPF) can be carried out arbitrarily from any of the inputs of the proposed MIBDCs to the outputs, but the existing MIBDCs can achieve IPF from the second input alone.

V. CONCLUSION

Using dual active bridge and phase-shifted full bridge topologies, an unique unidirectional multiport isolated dc to dc converter with bipolar symmetric outputs has been proposed in this study. Analysis and verification of the proposed MIBDC have been performed for two inputs with equal and unequal input voltages at various duty cycles. It was demonstrated how the MIBDC performed during the independent and concurrent power transfer from the sources to the dc link in both open and closed loop. Additionally, two crucial characteristics of bipolar converters—reliability under critical unipolar loads and natural symmetry of the dc link under unbalanced loads—were analysed and validated. The results presented in this paper show the validation on the in-house hardware-in-the-loop (HIL) platform. The suggested MIBDC can be used for energy harvesting in PV farms, mini-wind farms, and other dc-voltage-based renewable energy systems.

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IMMANUEL NINMA JIYA (Student Member, IEEE) received the B.Eng. degree in electrical and electronics engineering from the Federal University of Technology, Minna, Nigeria, in 2016, the M.Eng. degree in electrical and electronic engineering from North-West University, Potchefstroom, South Africa, in 2019, and the Ph.D. degree in renewable energy from the Faculty of Engineering and Science, University of Agder, Grimstad, Norway, in 2023.

From July 2022 to January 2023, he was a Guest Ph.D. Researcher with the Electronic and Intelligent (ELITE) Grid Research Laboratory, Department of Electrical and Computer Engineering, University of Alberta, Edmonton, Canada. His research interests include hardware-in-the-loop (HIL) and experimental design and control of new converter topologies and their applications to renewable energy and microgrid systems.

HUYNH VAN KHANG received the B.Sc. degree in electrical engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam, in 2002, the M.Sc. degree in electrical engineering from Pusan National University, Busan, South Korea, in 2008, and the D.Sc. (Tech.) degree in electrical engineering from Aalto University, Espoo, Finland, in 2012.

From 2013 to 2019, he was an Associate Professor in electrical power engineering with the University of Agder, Grimstad, Norway, where he is currently a Professor with the Department of Engineering Sciences. His research interests include electrical machines, condition-based maintenance, and applied power electronics.

PASAN GUNAWARDENA (Student Member, IEEE) received the B.Sc. degree in electrical engineering and M.Phil. degree in electronics and telecommunication engineering from the University of Moratuwa, Moratuwa, Sri Lanka, in 2015 and 2019, respectively.

He is currently pursuing the Ph.D. degree in energy systems with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. His current research interests include dc–dc converter topologies and dc microgrid systems. He was a recipient of the Second Prize of the IEEE IAS Renewable and Sustainable Energy Conversion Systems Committee Conference Paper Award, in 2021.

NAND KISHOR (Senior Member, IEEE) received the Ph.D. degree from the Indian Institute of Technology, Roorkee, India, in 2006.

From August 2013 to October 2013, he was a Marie Curie Experienced Researcher (Marie Curie Fellow) with the Department of Electrical Engineering, Aalto University, Espoo, Finland. He is currently a Professor with the Department of Engineering, Østfold University College, Norway. He has coedited two books, such as *Modelling and Dynamic Behaviour of Hydropower Plant* and *ICT for Electric Vehicle Integration with the Smart Grid*, (IET, U.K.). His research interests include AI applications in power systems dynamics and control, wireless sensor systems, distributed generation with renewable resources, WAMS, and smart grid technologies. He serves as an Associate Editor for IEEE Systems Journal, *IET Generation, Transmission and Distribution*, and *IET Renewable Power Generation*.

YUNWEI RYAN LI (Fellow, IEEE) received the B.Sc. degree in electrical engineering from Tianjin University, Tianjin, China, in 2002, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2006.

In 2005, he was a Visiting Scholar with Aalborg University, Denmark. From 2006 to 2007, he was a Postdoctoral Research Fellow with Ryerson University, Canada. In 2007, he was with Rockwell Automation Canada before he joined University of Alberta, Canada. He is currently a Professor and the Interim Chair with the Department of Electrical and Computer Engineering, University of Alberta. His research interests include distributed generation, microgrids, renewable energy, high-power converters, and electric motor drives. He was a recipient of the Nagamori Foundation Award, in 2022, and the Richard M. Bass Outstanding Young Power Electronics Engineer Award from IEEE PELS, in 2013. He served as the General Chair for the IEEE Energy Conversion Congress of Exposition (ECCE), in 2020. He serves as the Editor-in-Chief for IEEE Transactions on Power Electronics Letters. Prior to that, he was an Associate Editor for IEEE Transactions on Power Electronics, IEEE Transactions on Industrial Electronics, IEEE Transactions on Smart Grid, and IEEE Journal of Emerging and Selected Topics in Power electronics. He is an AdCom Member at Large for IEEE Power Electronics Society (PELS), from 2021 to 2023. He is recognized as a Highly Cited Researcher by the Clarivate Analytics.